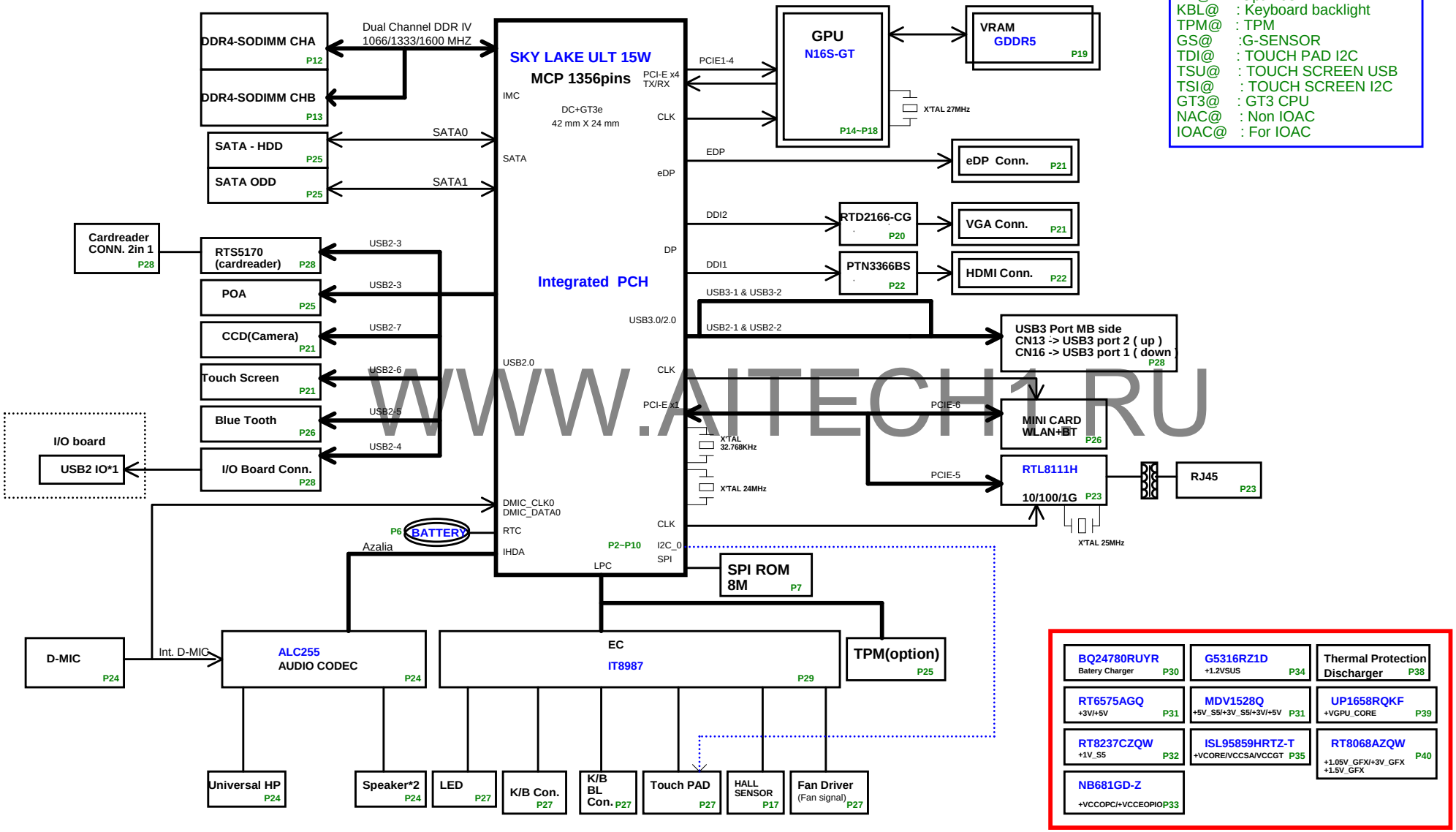
Z8V Serials SKL ULT SYSTEM BLOCK DIAGRAM

BOM

IV@ : iGPU
EV@ : Optimus
KBL@ : Keyboard backlight
TPM@ : TPM
GS@ :G-SENSOR
TDI@ : TOUCH PAD I2C
TSU@ : TOUCH SCREEN USB
TSI@ : TOUCH SCREEN I2C
GT3@ : GT3 CPU
NAC@ : Non IOAC
IOAC@ : For IOAC

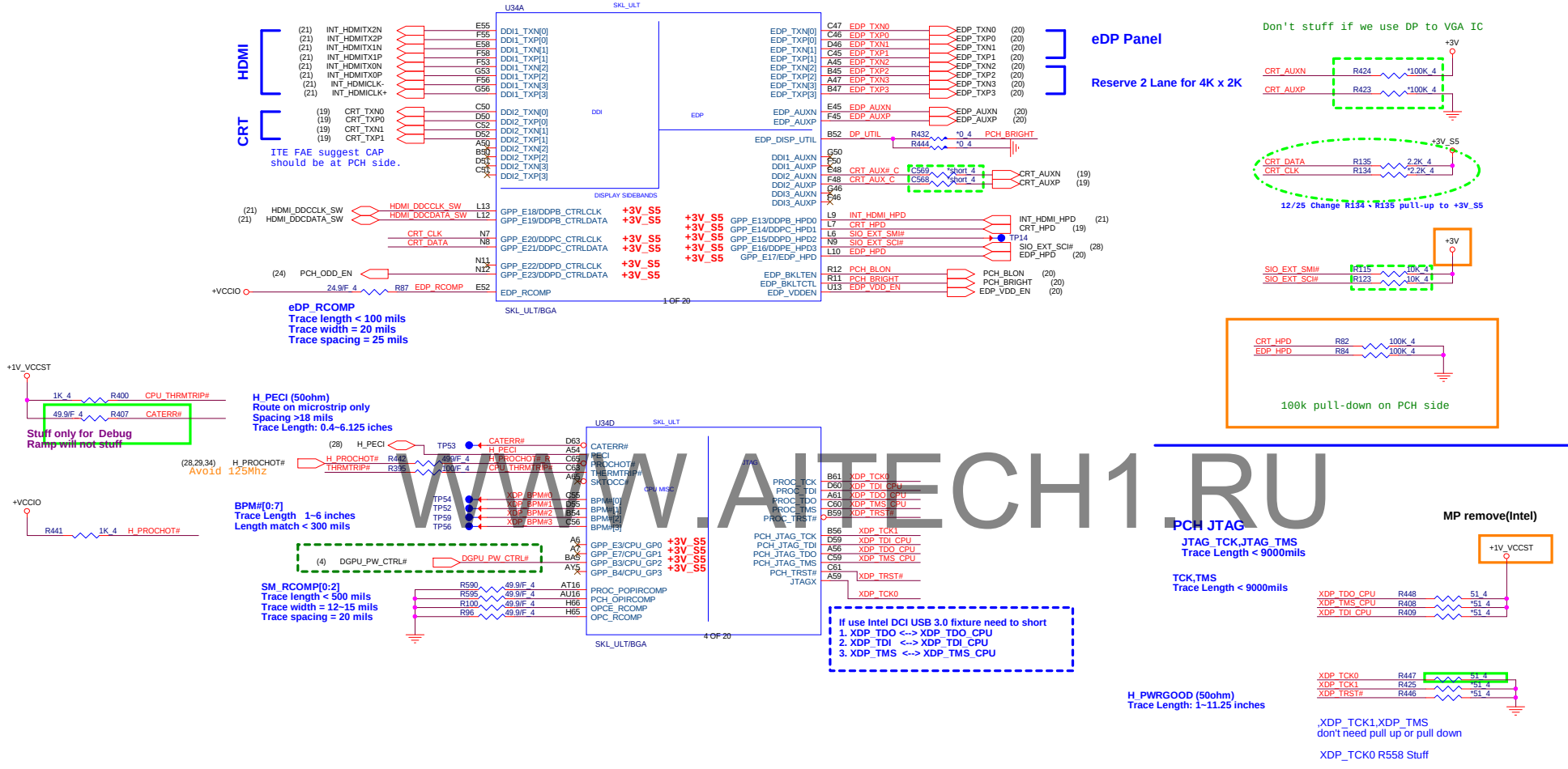


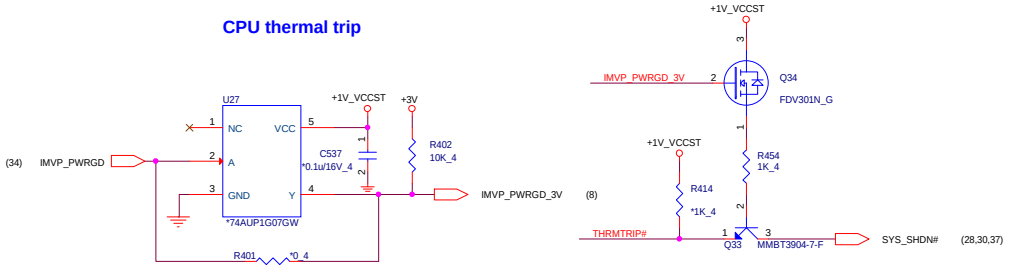
BQ24780RUYR Batery Charger P30	G5316RZ1D +1.2VSUS P34	Thermal Protection Discharger P38
RT6575AGQ +3V/+5V P31	MDV1528Q +5V_S5/+3V_S5/+3V/+5V P31	UP1658RQKF +VGPU_CORE P39
RT8237CZQW +1V_S5 P32	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P35	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P40
NB681GD-Z +VCCOPC/+VCCEOPIO P33		

Quanta Computer Inc.
PROJECT : ZRW
Block Diagram
Size | Document Number | Rev 1A
Date: Monday, February 22, 2016 Sheet 1 of 46

Skylake ULT (DISPLAY,eDP)

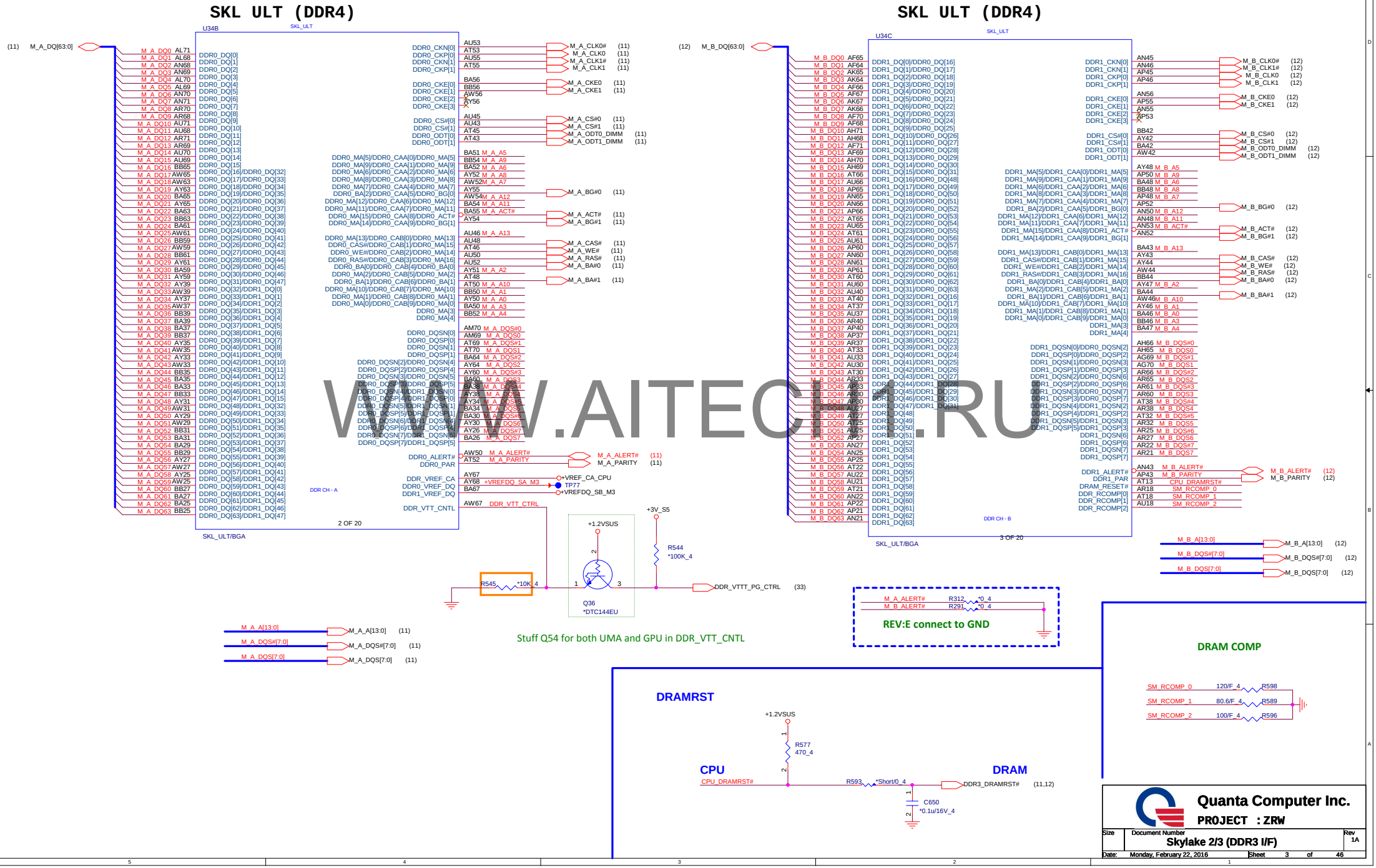
02





Quanta Computer Inc.			
PROJECT : ZRW			
Size	Document Number		Rev
	Skylake 1/4 (DDI/eDP)		1A
Date: Monday, February 22, 2016	Sheet 2	of 46	

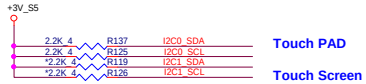
Change Data and DQS to interleave.



SKL ULT (SIDEBAND) GPIO

H_PECI (50ohm)
If route on microstrip,
Spacing need >18 mils
Trace Length: 2~15 iches

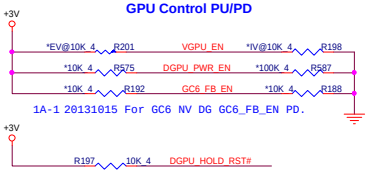
H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches



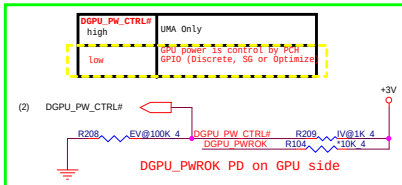
Touch PAD

Touch Screen

PU 2.2K for touch pad I2C bus(400 KHz)

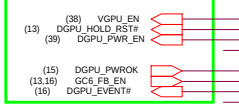


DGPU_PW_CTRL#	UMA Only
high	
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)



	DGPU_PW_CTRL#	VGA H/W Signal	Setup Menu	
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimise	0	GPU	Hidden	GPU boot

Add GPU Power Control Siganls

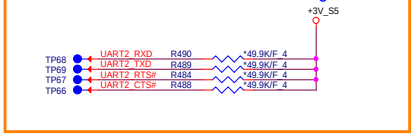


UART2 for RMT

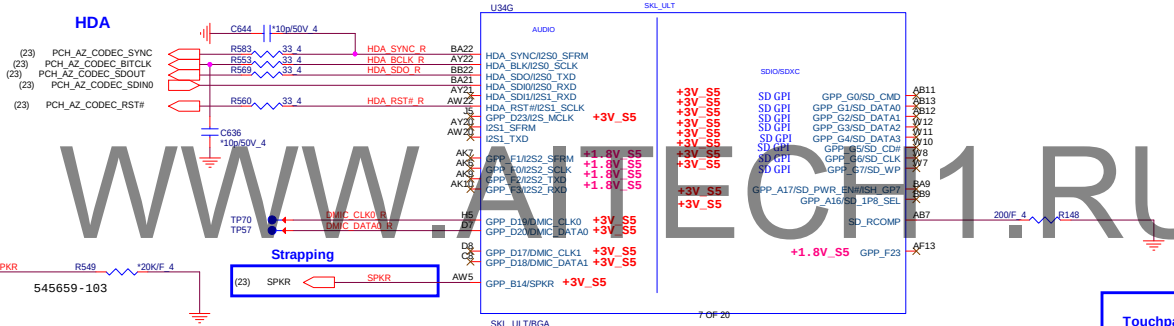
Touch PAD

Touch Screen

Reserve UART FFC TP for Win 7 debug



HDA



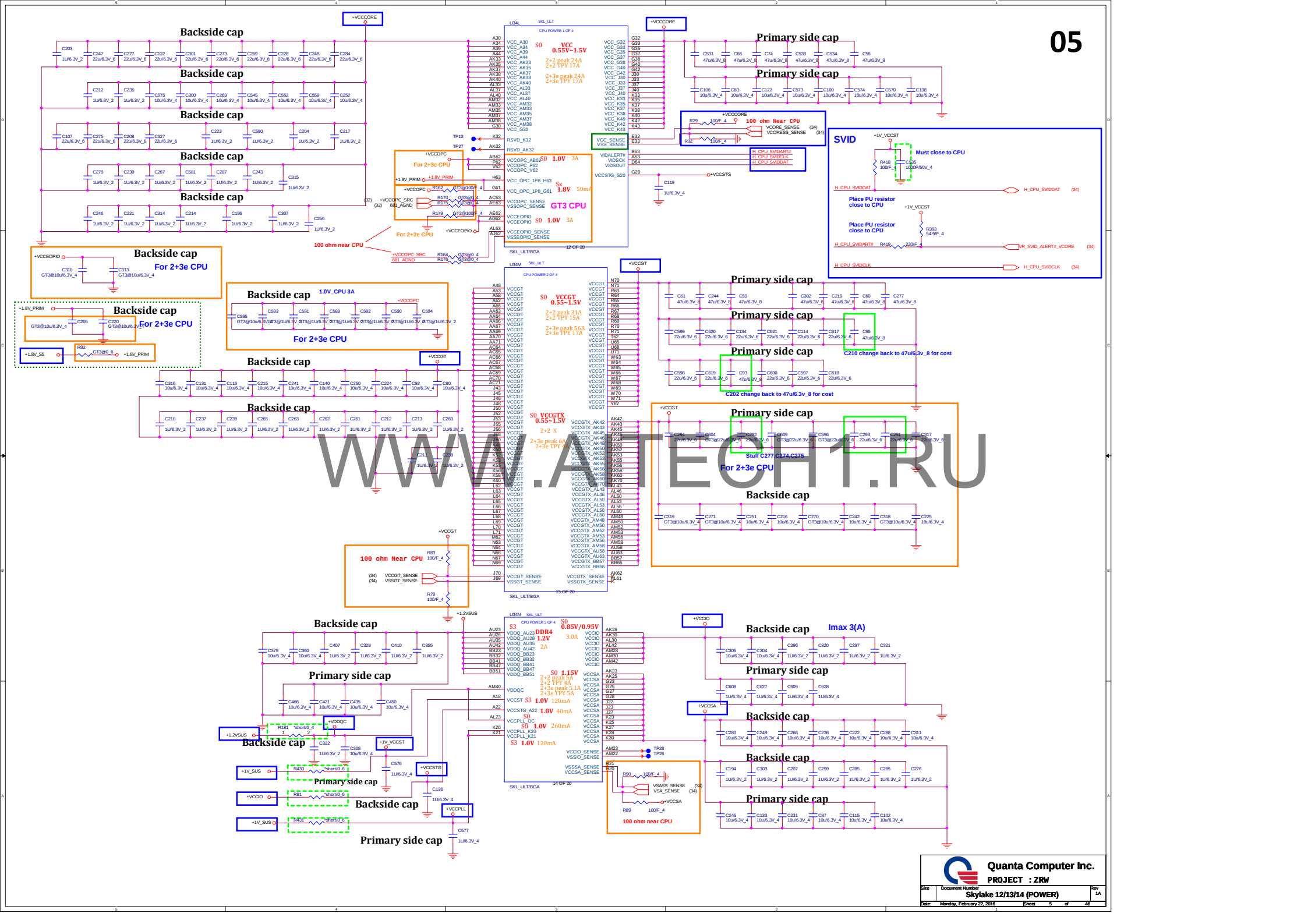
Strapping

Touchpad INT

Skylake-U Strapping Table

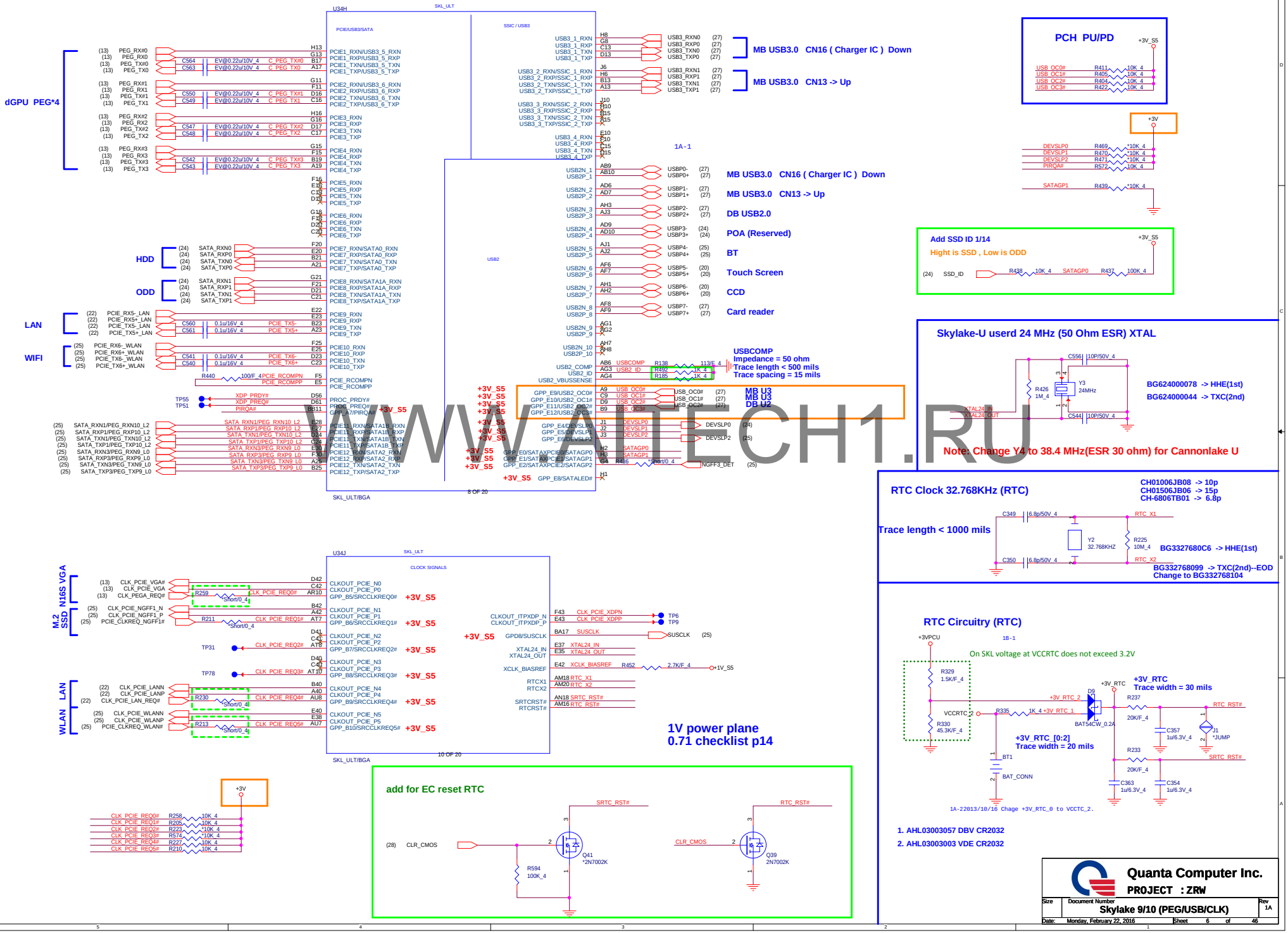
Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V R550 *1K_4 SPKR
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R543 *1K_4 GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) 1 = Enable Intel ME Cryp to TLS	+3V_S5 R144 *10K_4 SMBALERT# (7)
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R191 *1K_4 GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_S5 R481 *1K_4 SML0ALERT# (7)
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal HDA_SDO_R R570 *1K_4 ME_WR# (28)
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: Skylake 6/7 (PEG/DMI/FDI) | Rev 1A
Date: Monday, February 22, 2016 | Sheet 4 of 46

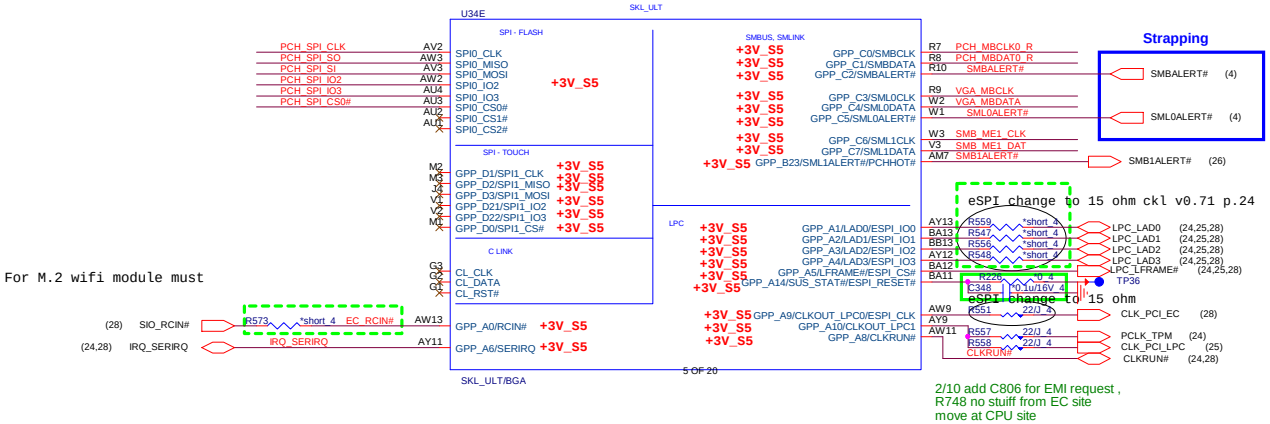


Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

06



Quanta Computer Inc. PROJECT : ZRW			
Size	Document Number: Skylake 9/10 (PEG/USB/CLK)		Rev 1A
Date: Monday, February 22, 2016	Sheet 6 of 46		



For M.2 wifi module must

eSPI change to 15 ohm ckl v0.71 p.24

eSPI change to 15 ohm

2/10 add C806 for EMI request , R748 no stuiff from EC site move at CPU site

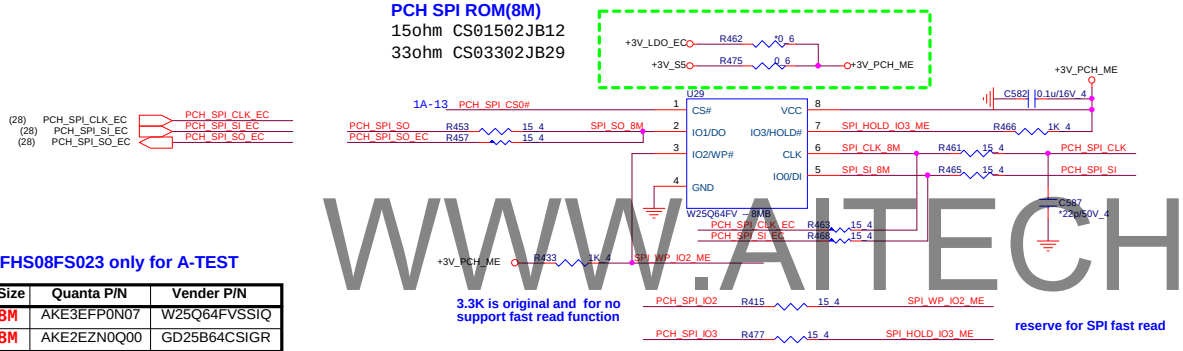
Strapping

SMBALERT# (4)
SML0ALERT# (4)
SMB1ALERT# (26)

SMBus

Termination Resistor Requirement for PCH PCHHOT# Pin
Reserve PU 150K resister

PCH SPI ROM(8M)
15ohm CS01502JB12
33ohm CS03302JB29



3.3K is original and for no support fast read function

reserve for SPI fast read

SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR

only 0ohm option

SMBus(PCH)

S5 — S0

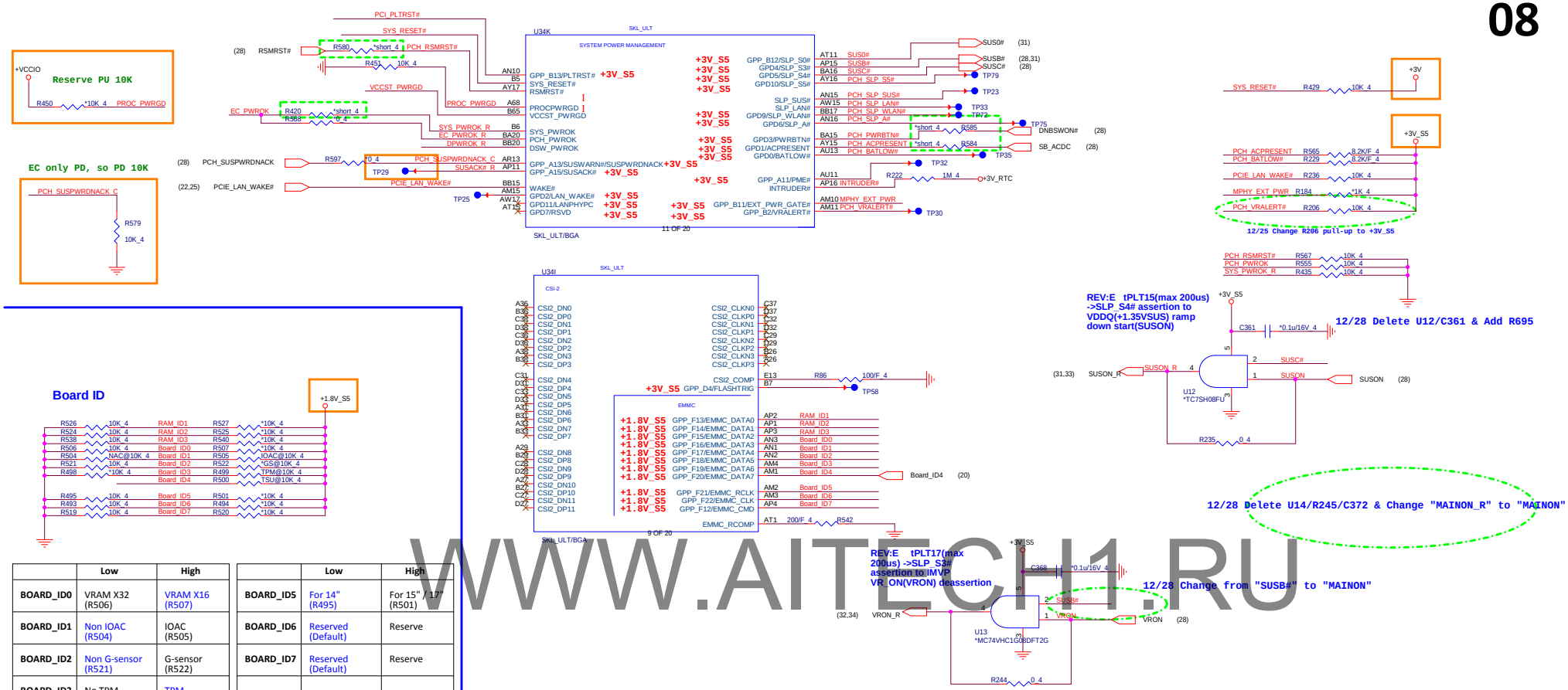
PCH_XDP_WLAN/S5 — DDR_TP/S0

Change to 2.2k

SMBus(EC)

EC/S5

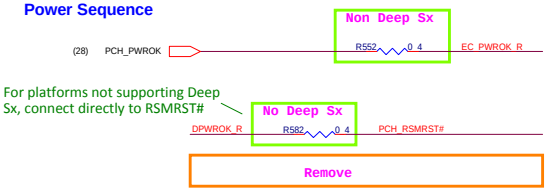
Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: Skylake 5 (SATA/HDA/SPI) | Rev 1A
Date: Monday, February 22, 2016 | Sheet 7 of 46



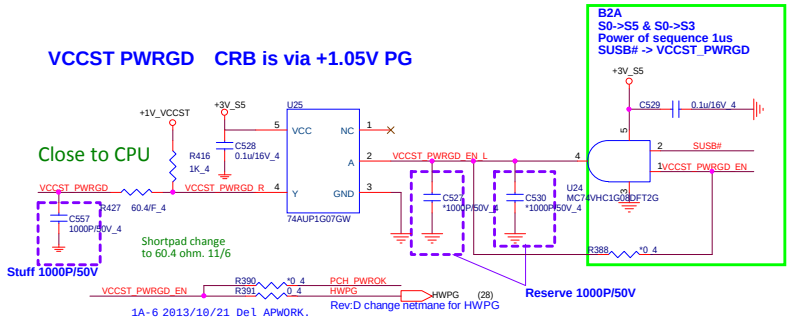
	Low	High
BOARD_ID0	VRAM X32 (R506)	VRAM X16 (R507)
BOARD_ID1	Non IOAC (R504)	IOAC (R505)
BOARD_ID2	Non G-sensor (R521)	G-sensor (R522)
BOARD_ID3	No TPM (R498)	TPM (R499)
BOARD_ID4	No-Touch panel	Touch panel (R500)

	Low	High
BOARD_ID5	For 14" (R495)	For 15" / 17" (R501)
BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID7	Reserved (Default)	Reserve

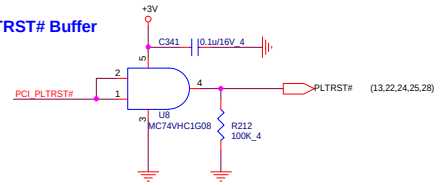
Power Sequence



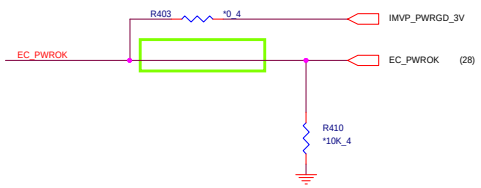
VCCST PWRGD CRB is via +1.05V PG



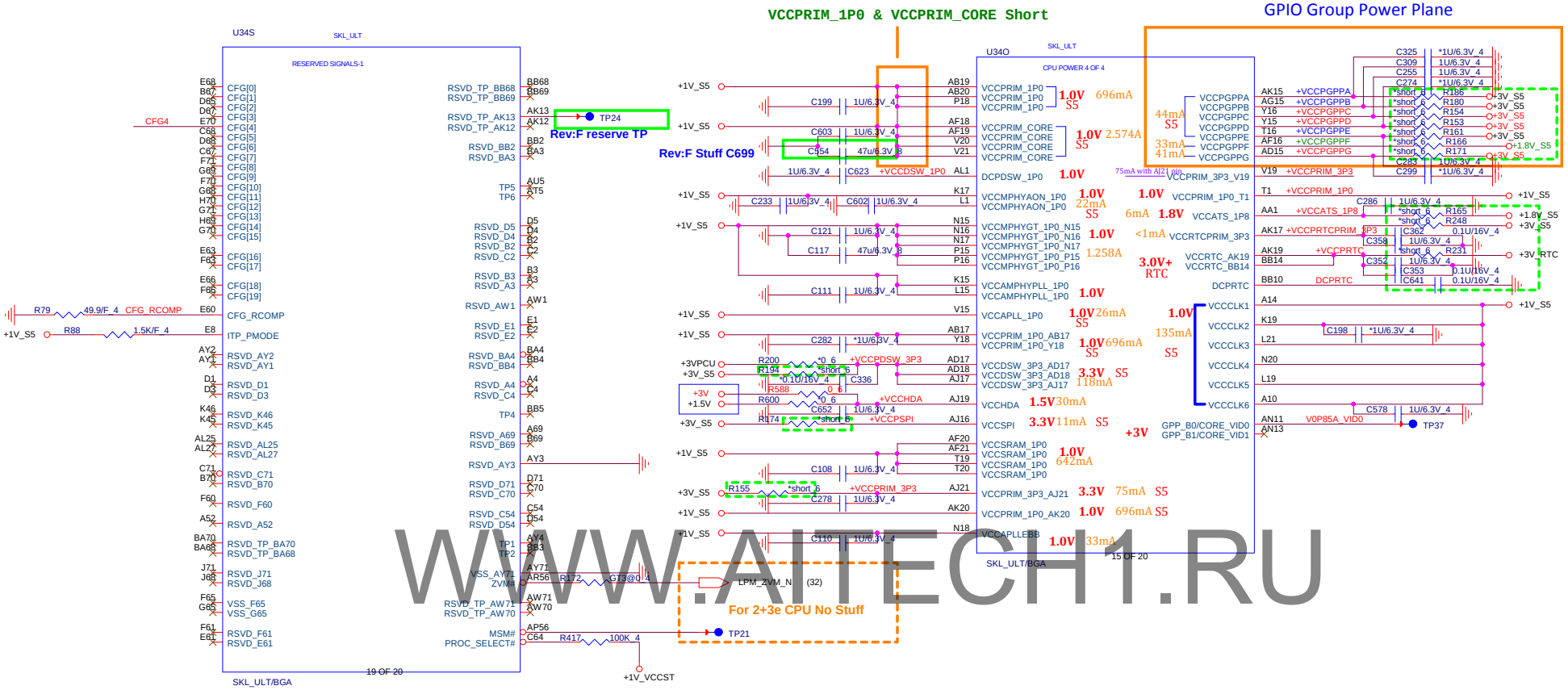
PLTRST# Buffer



SYSPWOK



Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: Skylake 9/11 (PWROK/Board_ID)	Rev: 1A
Date: Monday, February 22, 2016	Sheet 8 of 46	



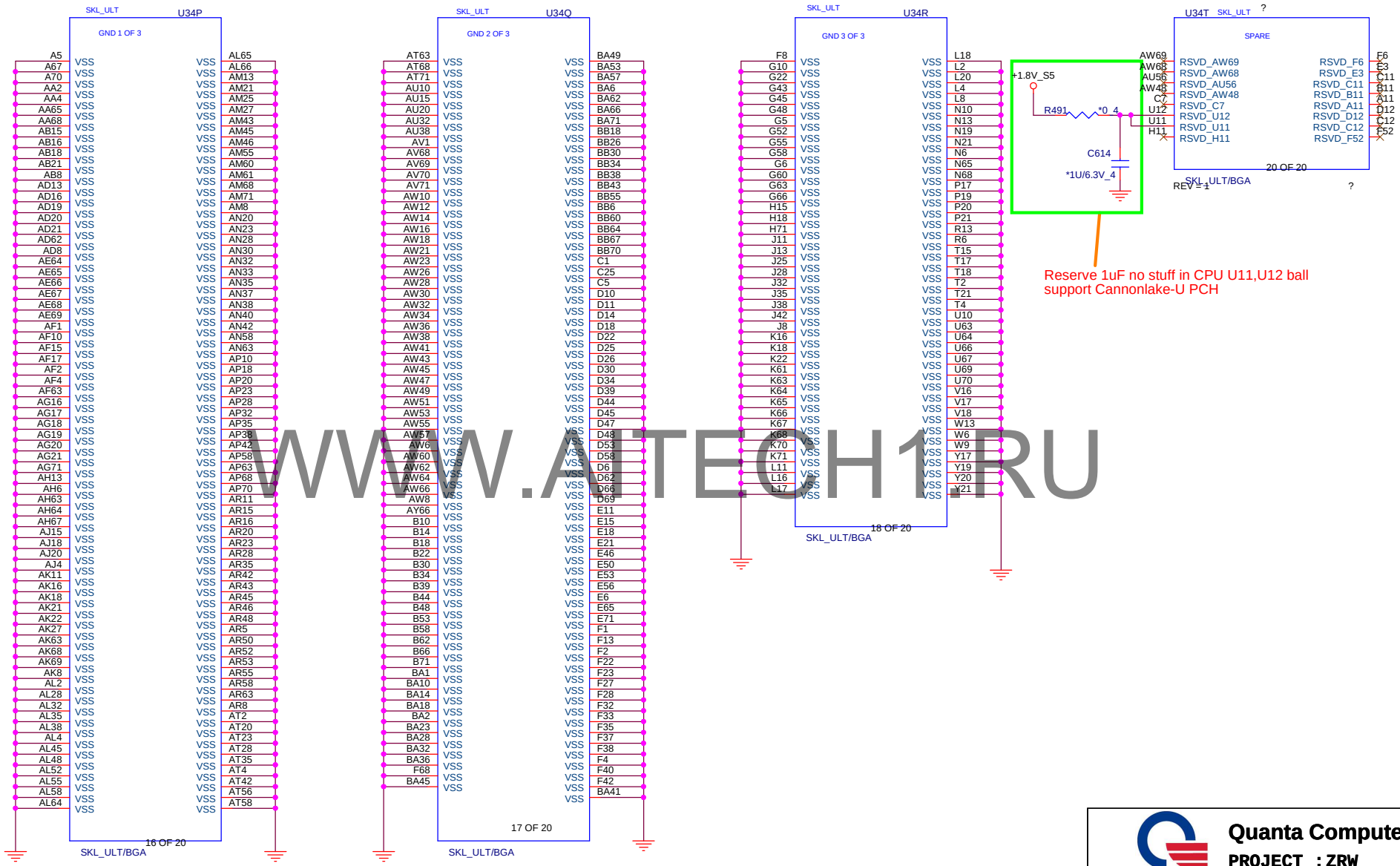
Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	**1 = *Normal Operation; No stall (iPU 3K)** 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	**1 = *Normal Operation(iPU 3K)** 0 = Lan number reversed	**H & S processor used only**
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) **0 = *Enabled**	CFG4 R455 1K_4
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	**H & S processor used only**
CFG[7]	PEG Training	**1 = *PEG Train immediatedly follow RESET# de-assertion (iPU 3K)** 0 = PEG wait for BIOS for training	**H & S processor used only**
CFG[19:8]	Reserved Configuration lane		

Quanta Computer Inc.
PROJECT : ZRW

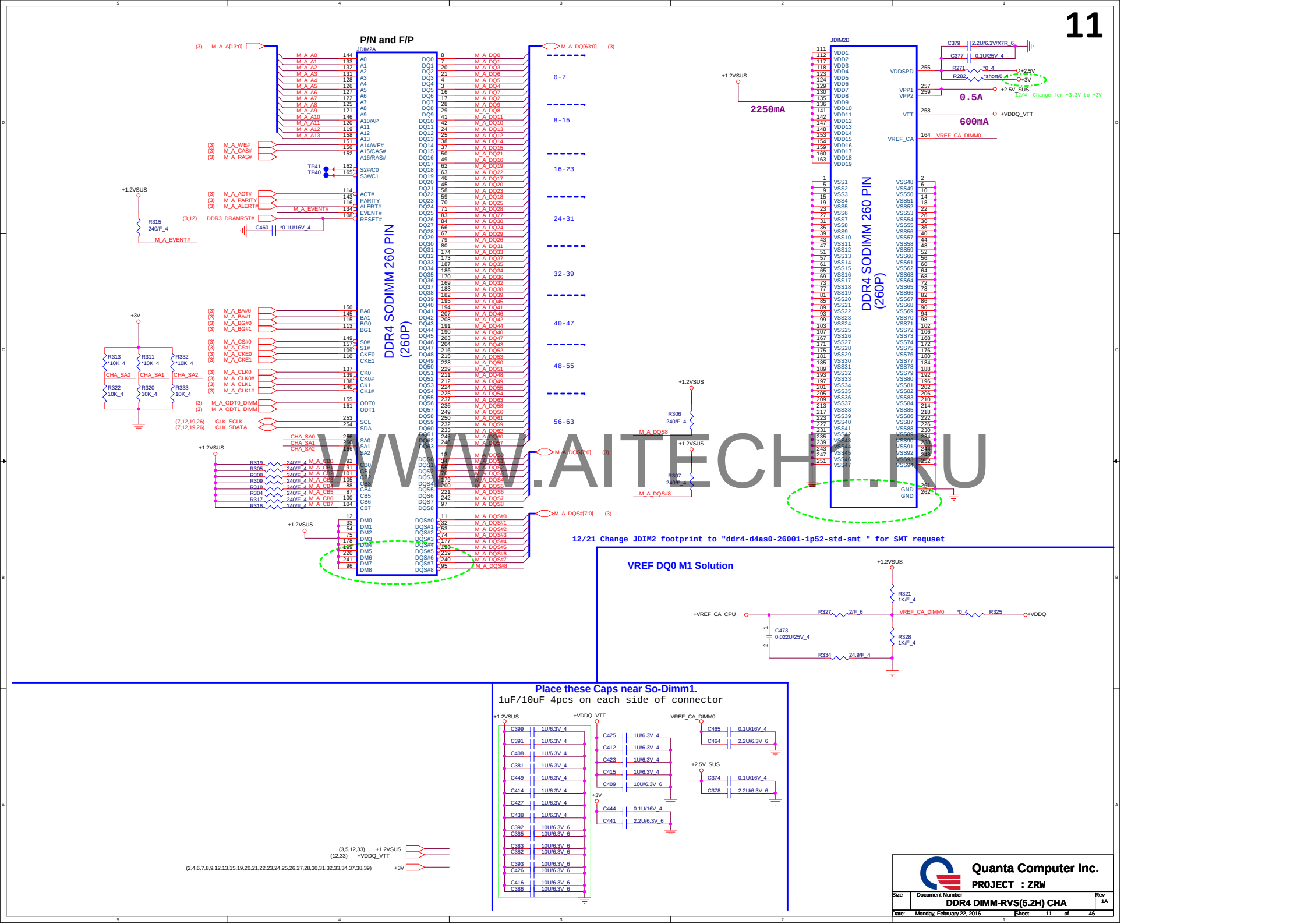
Size	Document Number	Rev
	Skylake PCH-LP 15/19 (POWER)	1A

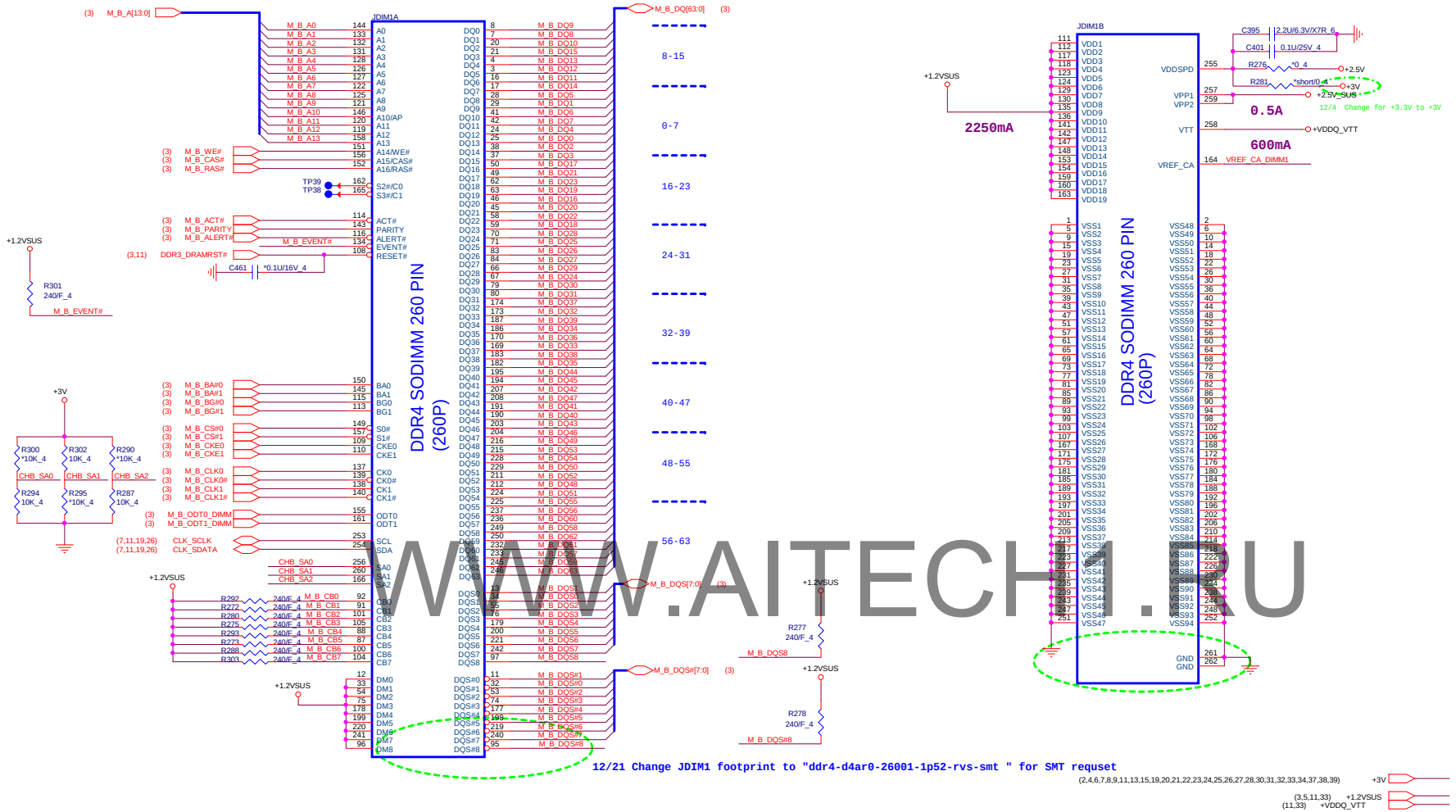
Date: Monday, February 22, 2016 Sheet 9 of 46

Skylake ULT (GND)

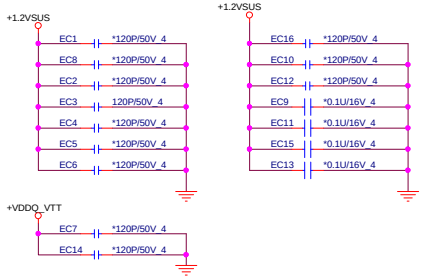


Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: Skylake 10/17/18 (GND)	Rev: 1A
Date: Monday, February 22, 2016	Sheet 10 of 46	



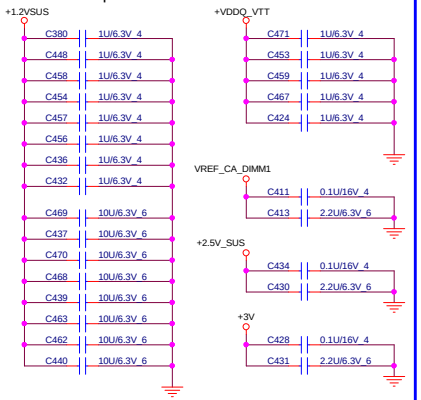


For EMI RESERVE

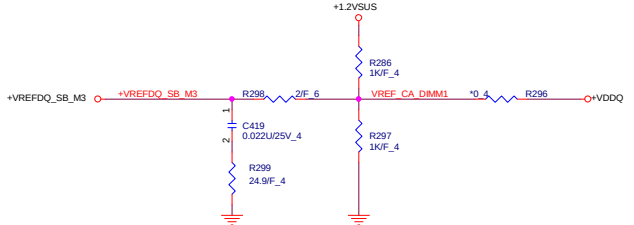


Place these Caps near So-Dimm0.

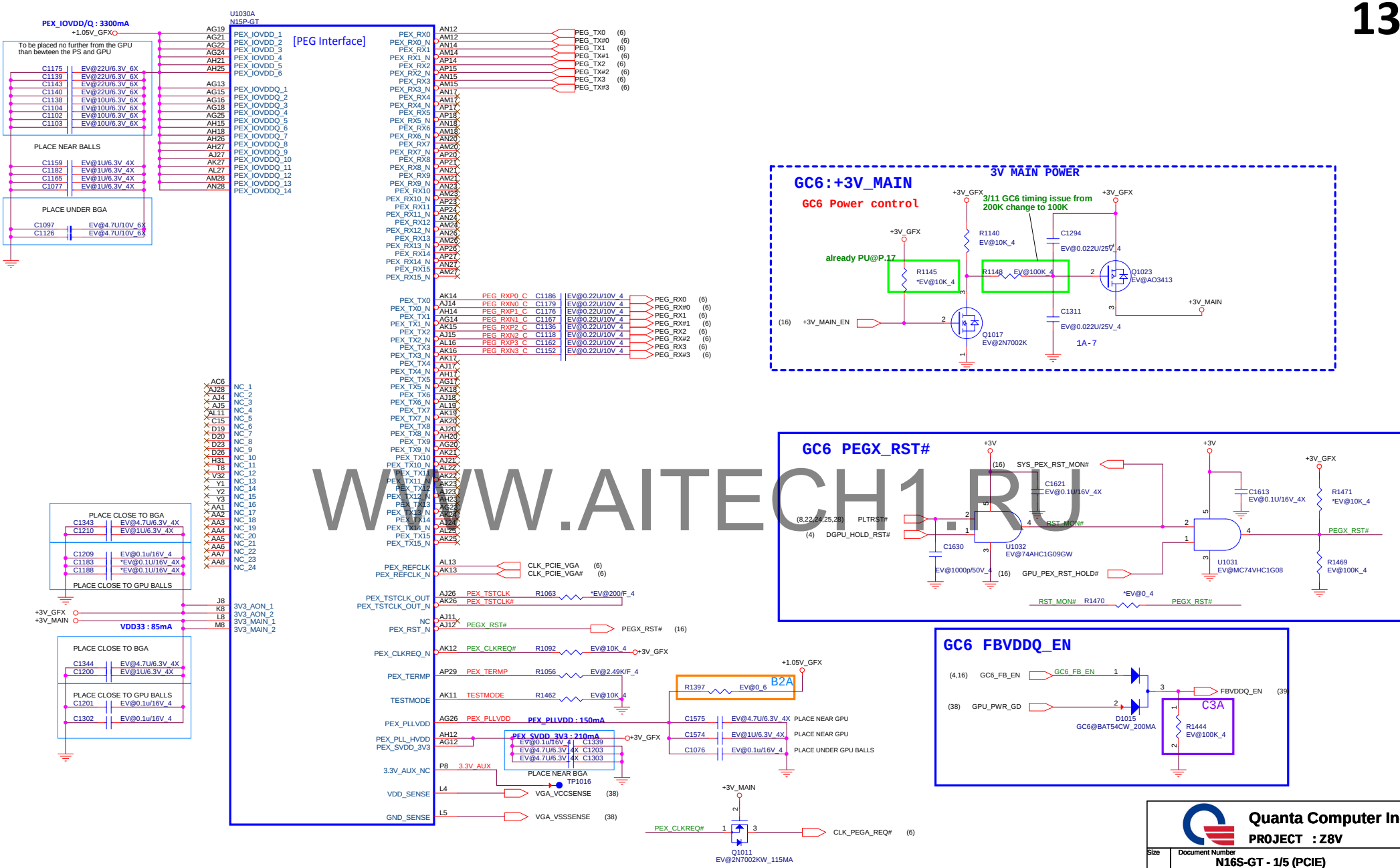
1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution



Quanta Computer Inc.			
PROJECT : ZRW			
Size	Document Number		Rev
	DDR4 DIMM-STD(5.2H) CHB		1A
Date: Monday, February 22, 2016		Sheet 12 of 46	



Quanta Computer Inc.		
PROJECT : Z8V		
Size	Document Number: N16S-GT - 1/5 (PCIE)	Rev: 1A
Date: Monday, February 22, 2016	Sheet 13 of 46	

U1030B N15P-GT

[MEMORY I/F A]

GDDR5 NO USE

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

U1030C N15P-GT

MEMORY I/F C

WCK only for GDDR5

C262 close to H27 (under GPU)

C574 close to K27 (under GPU)

C575 close to U27 (under GPU)

C576 near to GPU

Quanta Computer Inc.			
PROJECT : Z8V			
Size	Document Number		Rev
	N16S-GT - 2/5 (Memory)		1A
Date: Monday, February 22, 2016		Sheet 14 of 45	

U1030D
N15P-GT

[IFPA/B_LVDS]
AH8 IFPAB_PLLVDD
AG8 IFPA_IOVDD
AG9 IFPB_IOVDD
AJ8 IFPAB_RSET
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
AF7 IFPC_PLLVDD
AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
AG6 IFPD_IOVDD
AF8 IFPC_RSET
AN2 NC
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

[IFPE/F_DP]
AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
AC8 IFPF_IOVDD
AD6 IFPEF_RSET
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

[DACA/B_CRT]
AG10 DACA_VDD
AP9 DACA_VREF
AP8 DACA_RSET
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL
I2CA_SDA

[XTAL IN]
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN

(39) HWPG_1.35VGFX

R4 I2CA_SCL EV@1.8K/F_4 R1499
R5 I2CA_SDA EV@1.8K/F_4 R1129

H3 XTAL27_IN
H2 XTAL27_OUT
J4 XTAL_OUTBUFF R1147 EV@10K_4
H1 XTAL_SSIN R1523 EV@10K_4

3V_MAIN_PWGD

+3V_MAIN R1121 EV@4.7K_4 C1245 *1000p/50V_4
Q1019 EV@MMBT3904-7-F
+3V R1192 EV@4.7K_4 C1347 EV@1000p/50V_4
+3V_GFX R1184 EV@1.5K/F_4
Q1026 EV@DTC144EU
R1182 *100K/F_4
3V_MAIN_PWGD → 3V_MAIN_PWGD (38,39)

+1.05V_GFX and GPU core power EN

2/16 Reserve R1539 for DGPU_PWROK doesn't have any sequence requirement

R1539 *0_4
DGPU_PGOK-1
+3V_GFX
+3V
R1105 EV@4.7K_4
R1088 EV@4.7K_4
R1082 EV@4.7K_4 DGPU_POK2
Q1010 EV@METR3904-G
Q1012 EV@DTC144EUA
R1098 EV@100K/F_4
C1187 *1000P/50V_4
C1181 EV@1000P/50V_4
DGPU_PWROK (4)

PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS

+1.05V_GFX L1006 EV@HCB1005KF-330T30
C1253 EV@22U/6.3V_6X
NV_PLLVDD AD8
PLLVDD : 200mA
B2A
C1213 EV@0.1U/16V_4X
PLLVDD
AE8 SP_PLLVDD
C5092 Close to AE8
C5090 Close to AD7
+1.05V_GFX L1005 EV@HCB1005KF_1.5A
C1242 EV@22U/6.3V_6X
C1204 EV@4.7U/6.3V_4X
AD7 VID_PLLVDD
B2A
C1214 EV@0.1U/16V_4X
C1231 EV@0.1U/16V_4X

Reserve
+3V_GFX
XTAL_OUTBUFF R1146 *EV@10K_4

BG627000039 -> HHE(1st)
BG627000035 -> TXC(2nd)

XTAL27_IN
XTAL27_OUT
Y1004
EV@27MHZ_10
C1637 EV@10P/50V_4C
C1638 EV@10P/50V_4C
B2A

Quanta Computer Inc.
PROJECT : Z8V
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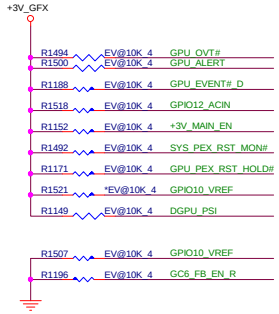
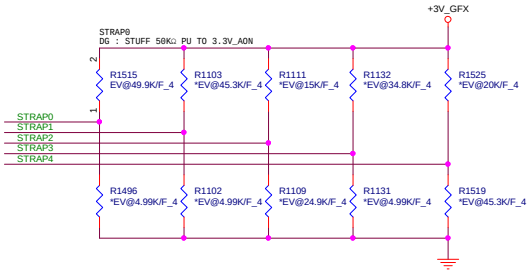
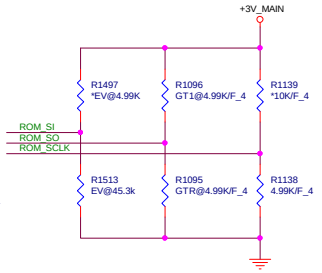
Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18 GM
49.9K ---> CS34992FB10 GT

	Package	DevID
N16S-GT1-KB	GB4b-128	0x179C
N16S-GTR	GB4b-128	0x134D





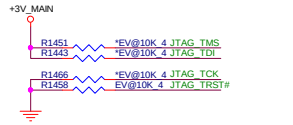


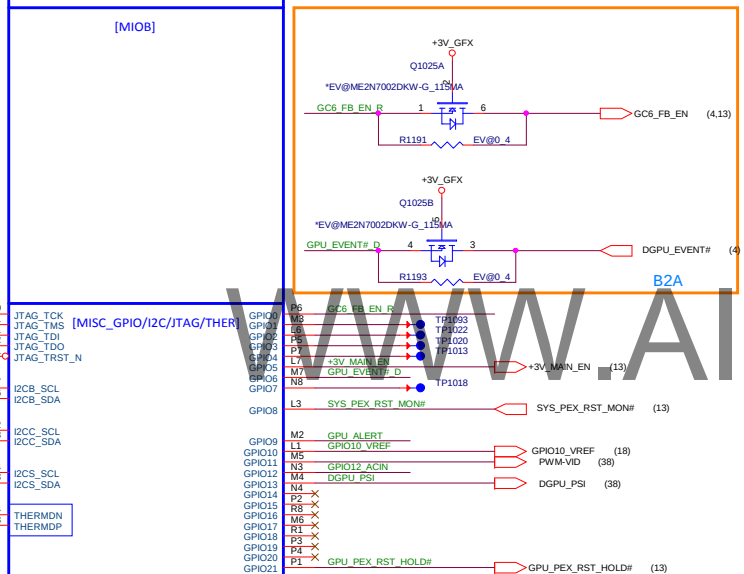
	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

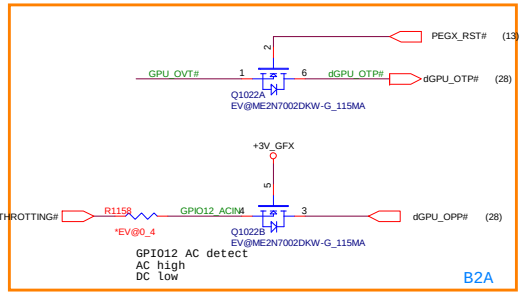
Mutil-level mode strapping:
For N16S-GT1-KB-A2 :
R490=40.2k PD
1.ROM_SCLK =4.99K PD
2.ROM_SO = 4.99K PU (N16S-GTR = 4.99KPD)
3.ROM_SI= Memory strap setting
4.STRAP0 = 49.9k PU
5.Strap4~1 = Reserve Pull up and Pull down

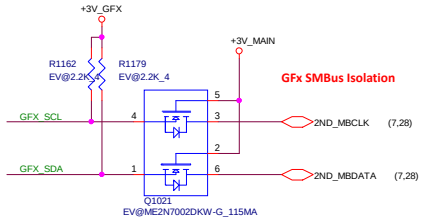
	N16S-GT1-KB-A2	N16S-GTR
ROM_SO	R93 PU 4.99K	R92 PD 4.99K
ROM_SI	As below configuration table	

Reserve PU/PD for Debug









N16S-GT1-KB-A2 VRAM Configuration Table:

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x8) 0001 (0x9)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull up 10K Pull up
8GbX4 (4GB)	0000 (0x8) 0001 (0x9)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull up 10K Pull up

N16S-GTR VRAM Configuration Table:

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull down 10K Pull down
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull down 10K Pull down

N16S-GT1-KB-A2 (GB4b-128)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0000
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND [Stuff 49.9K PU]				0001
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND [Do Not Stuff				
STRAP2					
STRAP3					
STRAP4					

Quanta Computer Inc.
PROJECT : Z8V
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VDD/XVDD : 43A

+VGPU_CORE

U1030F
N15P-GT

[GPU VDD]

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_026	Y4
M23	VDD_024	XVDD_027	Y5
N13	VDD_025	XVDD_028	Y6
N15	VDD_026	XVDD_029	Y7
N17	VDD_027	XVDD_030	Y8
N18	VDD_028		
N20	VDD_029		
N22	VDD_030		
P12	VDD_031		
P14	VDD_032		
P16	VDD_033		
P19	VDD_034		
P21	VDD_035		
P23	VDD_036		
R13	VDD_037		
R15	VDD_038		
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

+VGPU_CORE

U1030G
N15P-GT

[GPU GND]

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	R21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN30	GND_79	GND_179	U21
AN34	GND_80	GND_180	U23
AN4	GND_81	GND_181	V12
AN7	GND_82	GND_182	V14
AP2	GND_83	GND_183	V16
AP33	GND_84	GND_184	V19
B1	GND_85	GND_185	V21
B10	GND_86	GND_186	V23
B22	GND_87	GND_187	W13
B25	GND_88	GND_188	W15
B28	GND_89	GND_189	W17
B31	GND_90	GND_190	W18
B34	GND_91	GND_191	W20
B4	GND_92	GND_192	W22
B7	GND_93	GND_193	W28
C10	GND_94	GND_194	Y12
C13	GND_95	GND_195	Y14
C19	GND_96	GND_196	Y16
C22	GND_97	GND_197	Y19
C25	GND_98	GND_198	Y21
C28	GND_99	GND_199	Y23
C7	GND_100	GND_200	AH11
		GND_OPT_1	C16
		GND_OPT_2	W32

+VGPU_CORE

PLACE UNDER GPU

C1158	EV@1U/6.3V_4X	
C1206	EV@1U/6.3V_4X	
C1114	EV@1U/6.3V_4X	
C1094	EV@1U/6.3V_4X	
C1091	EV@1U/6.3V_4X	
C1089	EV@1U/6.3V_4X	
C1092	EV@1U/6.3V_4X	
C1160	EV@1U/6.3V_4X	
C1168	EV@4.7U/6.3V_6X	
C1197	EV@4.7U/6.3V_6X	
C1172	EV@4.7U/6.3V_6X	
C1098	EV@4.7U/6.3V_6X	
C1166	EV@4.7U/6.3V_6X	
C1196	*EV@4.7U/6.3V_6X	B2A
C1112	EV@4.7U/6.3V_6X	
C1267	EV@4.7U/6.3V_6X	
C1099	EV@4.7U/6.3V_6X	
C1180	*EV@4.7U/6.3V_6X	B2A
C1142	EV@4.7U/6.3V_6X	
C1170	*EV@4.7U/6.3V_6X	B2A
C1205	*EV@4.7U/6.3V_6X	
C1133	EV@4.7U/6.3V_6X	
C1122	EV@4.7U/6.3V_6X	

PLACE NEAR GPU

C1131	2	1 EV@22U/6.3V_6X	B2A
C1111	2	1 EV@22U/6.3V_6X	
C1190	2	1 EV@22U/6.3V_6X	
C1171	2	1 EV@22U/6.3V_6X	
C1155	2	1 EV@22U/6.3V_6X	
C1173	2	1 EV@22U/6.3V_6X	
C1177	2	1 EV@22U/6.3V_6X	
C1189		EV@4.7U/10V_6X	
C1184		EV@4.7U/10V_6X	
C1639		*EV@4.7U/10V_6X	B2A
C1277		EV@4.7U/10V_6X	
C1185		EV@4.7U/10V_6X	
C1641		330u/2V_7343	

Quanta Computer Inc.
PROJECT : Z8V

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	N16S-GT - 5/5 (Power)	1A

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CHANNEL A: 1G/2G GDDR5x32

(14) VMA_DQ[63..0] — VMA_DQ[63..0]
(14) FBA_DBI[7..0] — FBA_DBI[7..0]
(14) FBA_EDC[7..0] — FBA_EDC[7..0]

Channel 0 <0-31>

MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7

LOWER HALF

Channel 0 <32-63>

MF=1 mirrored

QD32~39
QD40~47
QD48~55
QD56~63

U1022 — EV@GDDR5 — U1022

U1021 — EV@GDDR5 — U1021

+1.35V_GFX

VREF_VMA1_MOS — VREF_VMA1_MOS — VREF_VMA2_MOS — VREF_VMA2_MOS

VMA_CLK0 — VMA_CLK1 — VMA_CLK0# — VMA_CLK1#

Q1034 EV@2N7002K — GPIO10_VREF (16)

CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.

20120117 Add C764 for EMI suggestion.

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

Quanta Computer Inc.
PROJECT : Z8V
Size — Document Number: N13PGV GDDR5x32-VRAM — Rev: 1A
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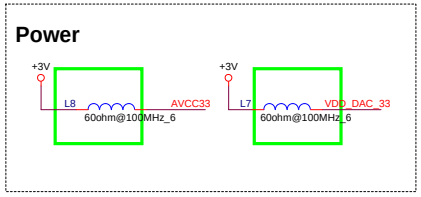
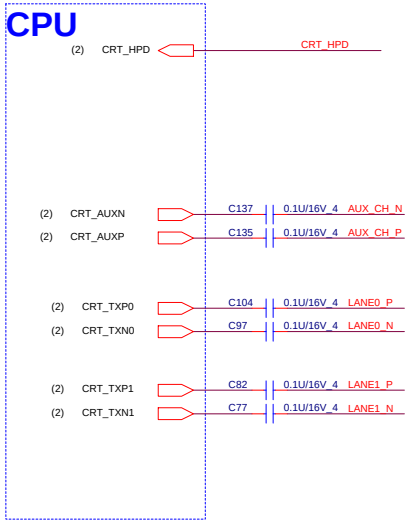
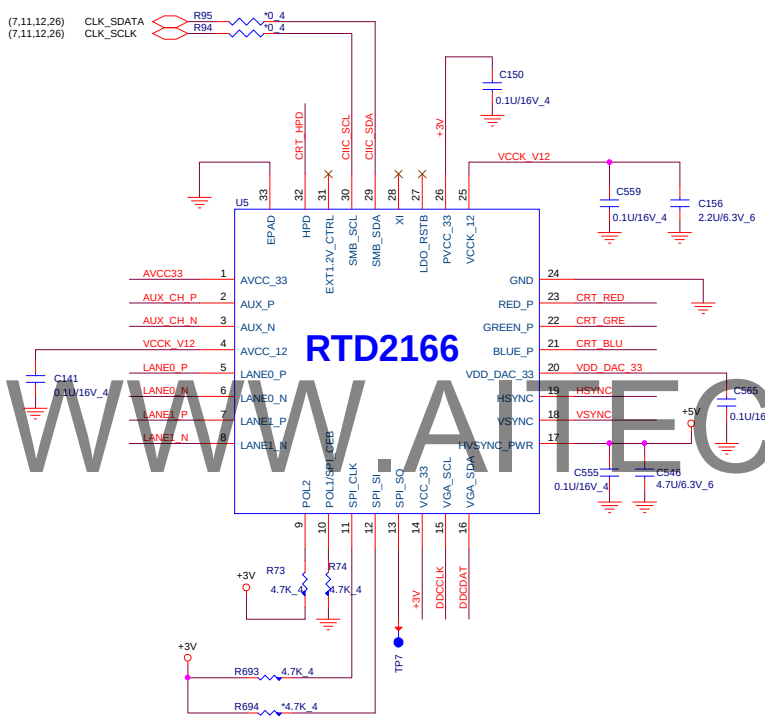
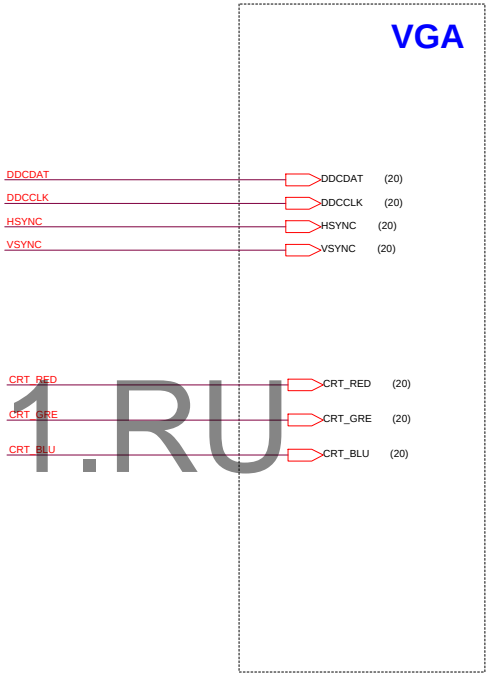
DP TO VGA









Note:

1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
2- C5 shold be X5R material
3- R6, R7, R8 should be 75 ohm with +/-1%
4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
5- This configuration is for internal ROM mode and using embedded LDO mode.

(2,4,6,7,8,9,11,12,13,15,20,21,22,23,24,25,26,27,28,30,31,32,33,34,37,38,39) +3V
(20,21,23,24,26,30,37) +5V

Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	DP to VGA iT6165	1A
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CRT

RTD2166 integrate 5V HSYNC/VSYNC buffer inside IC

12/24 Delete R449

12/18 Change R412 to 47ohm for vendor requset

12/24 Delete R396

12/18 Change R399 to 47ohm for vendor requset

Co-Layout

Realtek FAE suggest close to connector

12/18 Change to BLM15BB220SN1D (CX5BB220005) for vendor request

Close to RTD2166 IC

12/18 Un-Stuff C95/C128/C148 for vendor requset

12/21 Change CN5 footprint to "dsub-95-0005-01-15p" for layout requset

12/18 Un-Stuff C539/C551 for vendor requset

Realtek FAE suggest close to connector

Power trace tracking

LCD CONNECTOR

2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage

Prevent ESD/EOS Layout near device

eDP FHD

Touch Panel-I2C

Touch Panel-USB

eDP 4k*2k

CCD-USB

MAX 1.5A

S5

Prevent ESD/EOS Layout near device

1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.

Touch Panel interrupt

S5 S0

LCD Power

1st : AL005245000---GMT
2nd : AL007553000---UPI

Touch screen level shift I2C(reserve)

S5 S0

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.

LID591#,EC intrnal PU

1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

Hall Sensor (HSR)

1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

Quanta Computer Inc.
PROJECT : ZRW

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	CRT/LVDS/CAMERA/LID	1A

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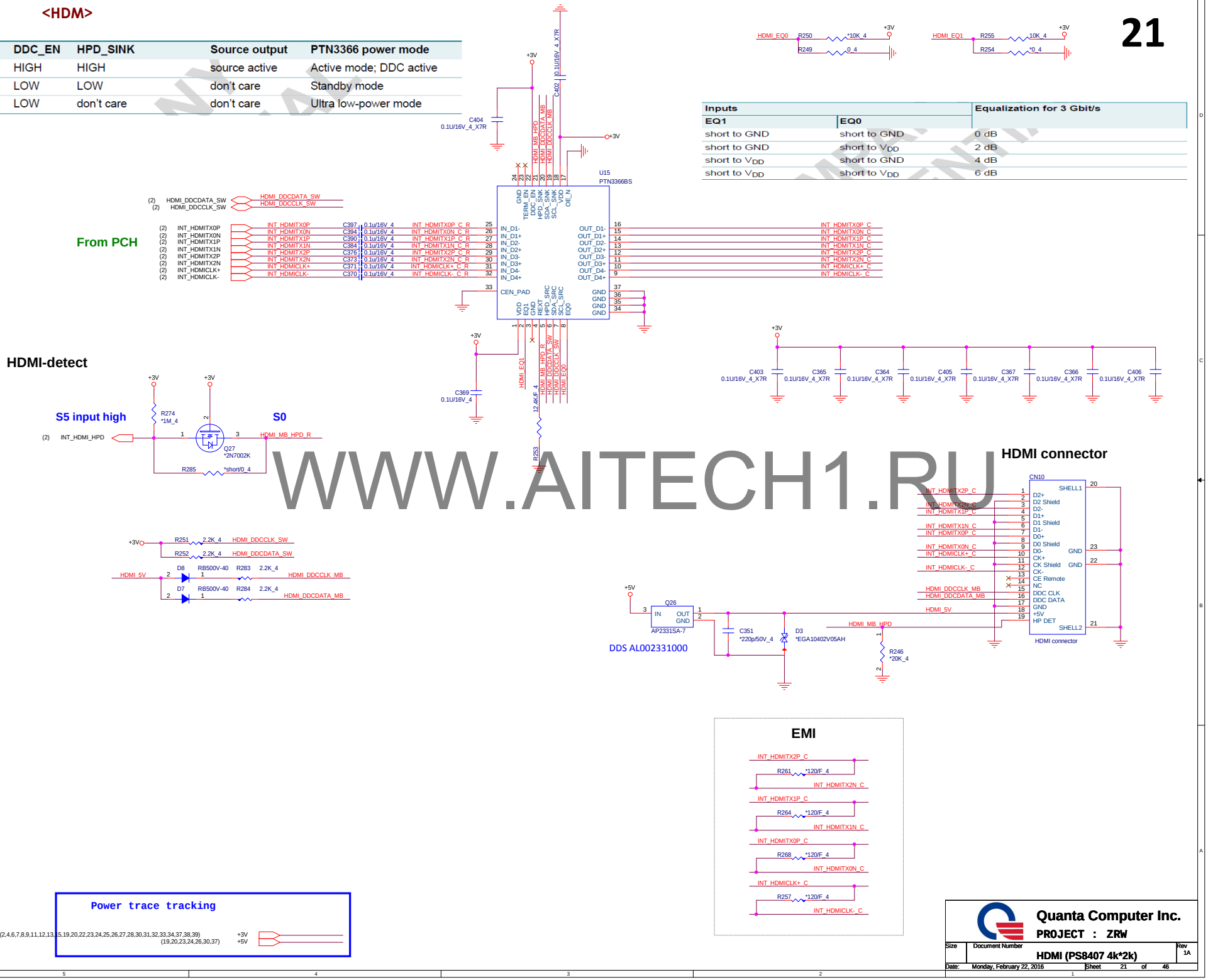
HDMI

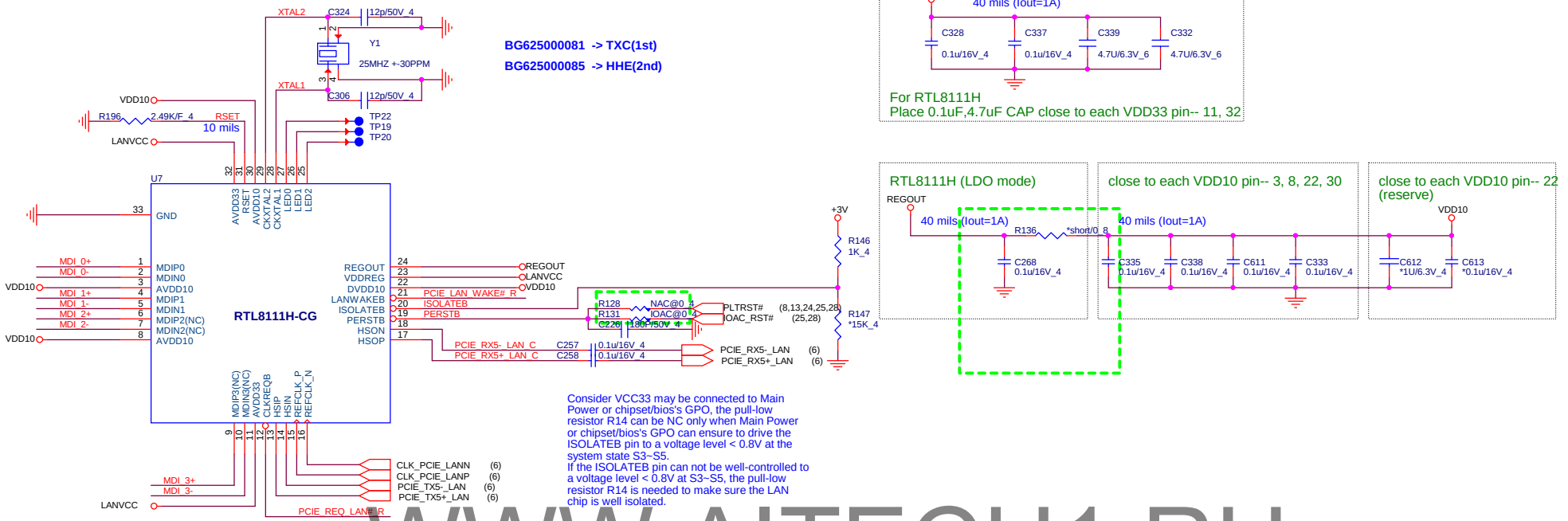
<HDM>

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

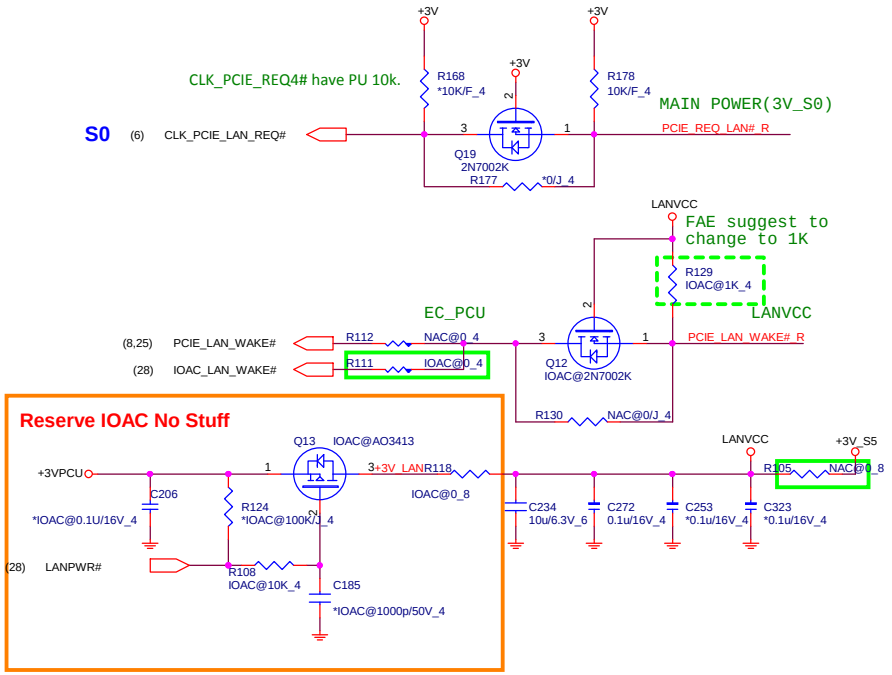
Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB



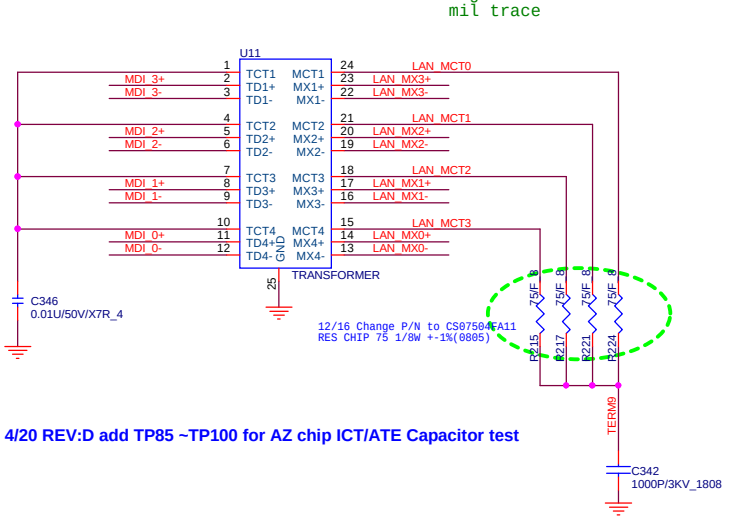
Giga LAN (LAN)



Leakage circuit (MPC)

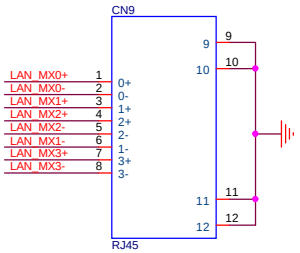


Tramsformer



4/20 REV:D add TP85 ~TP100 for AZ chip ICT/ATE Capacitor test

RJ45 Connector



Quanta Computer Inc.			
PROJECT : ZRW			
Size	Document Number		Rev
	LAN(RTL8111H)		1A
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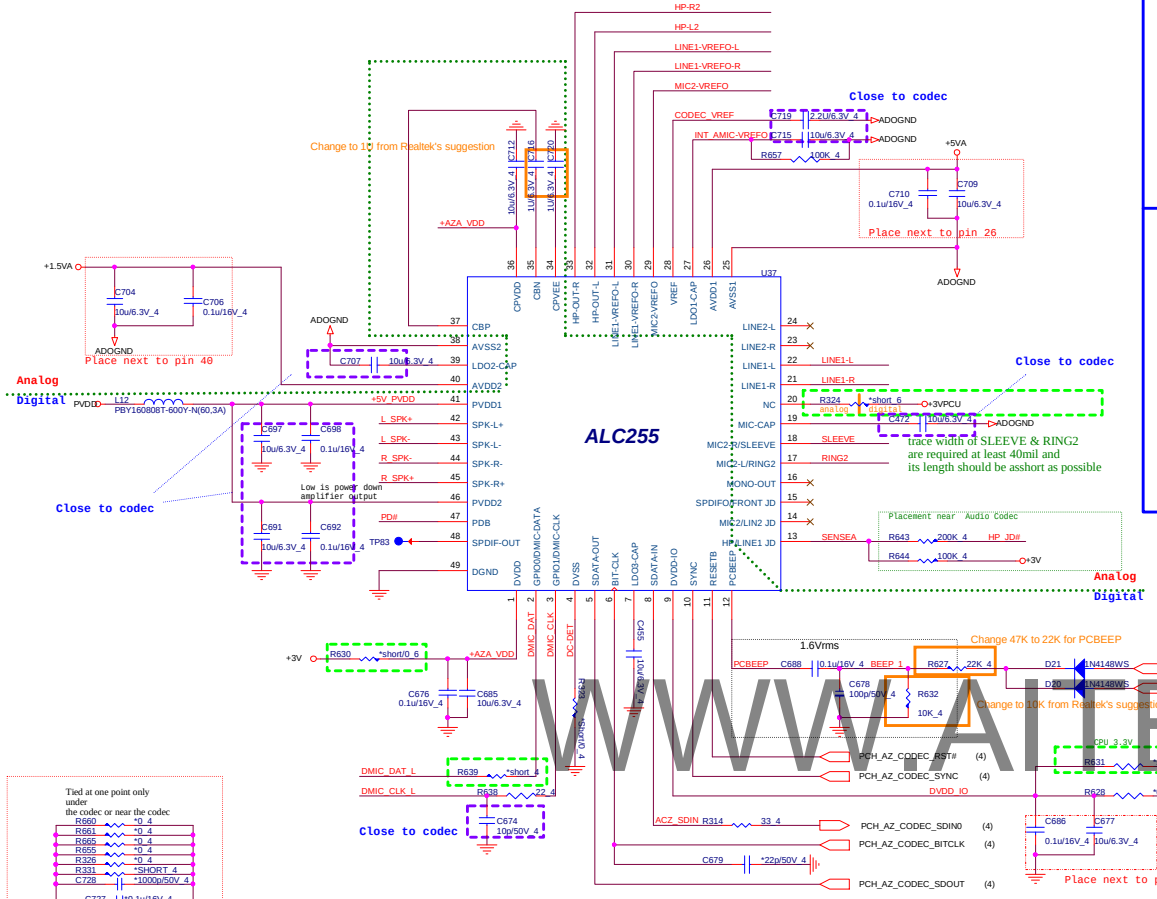
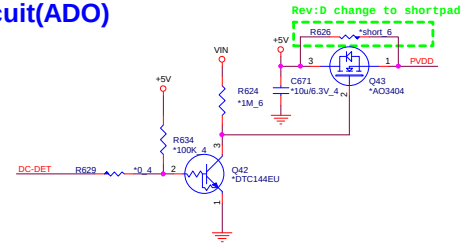
Codec(ADO)

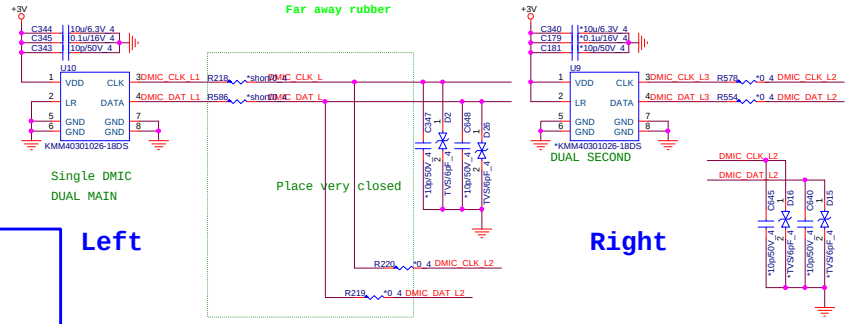


DC-DET circuit(ADO)



D-Mic (MIC)

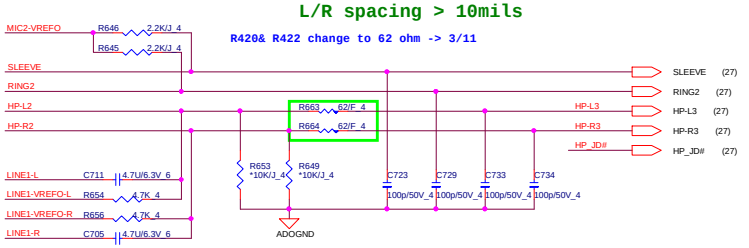
Single DMIC and Dual DIMC same PN: AL403010A00



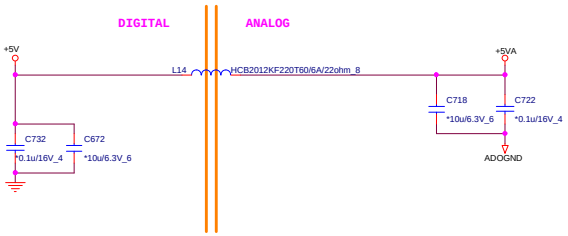
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils

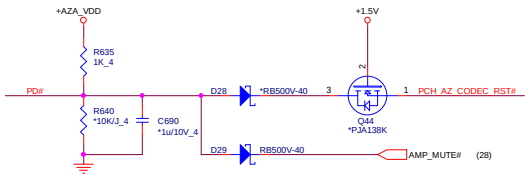
R420& R422 change to 62 ohm -> 3/11



Codec PWR 5V(ADO)

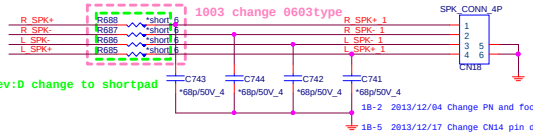


Mute(ADO)

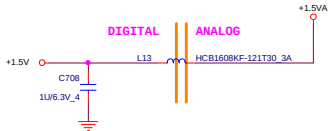


Internal Speaker

40mil for each signal 4 ohm : 40mil for each signal



Codec PWR 1.5V(ADO)



Quanta Computer Inc.
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	ALC255/HP/SPK	1A
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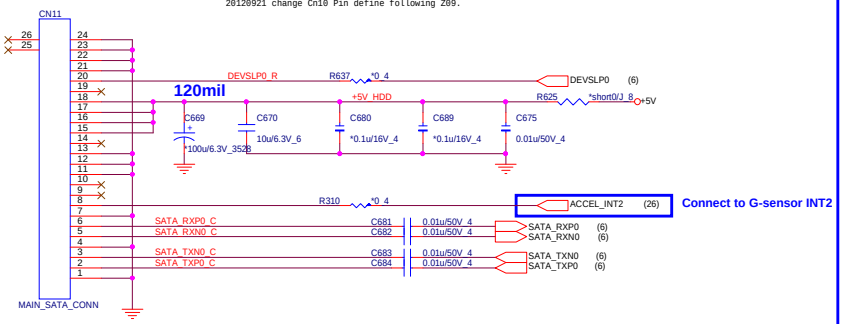
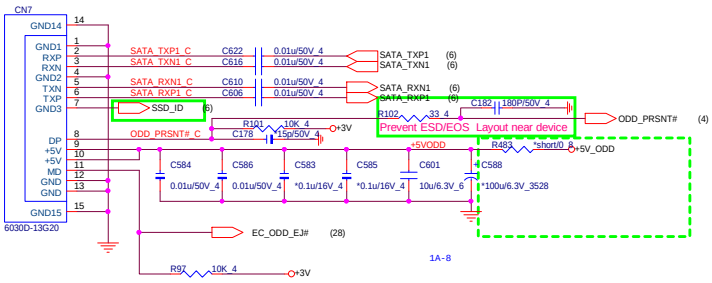
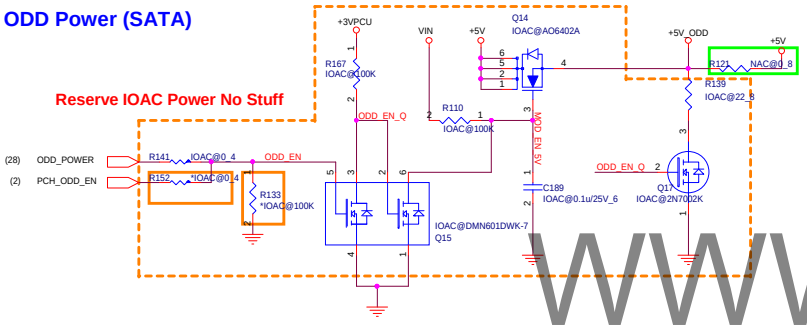
SATA HDD



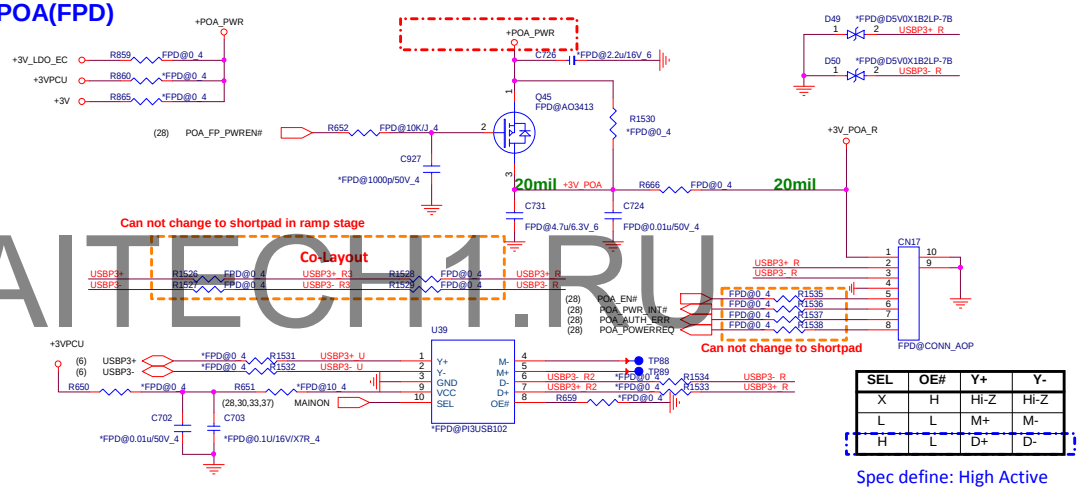
SATA ODD Connector



ODD Power (SATA)



POA(FPD)



SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

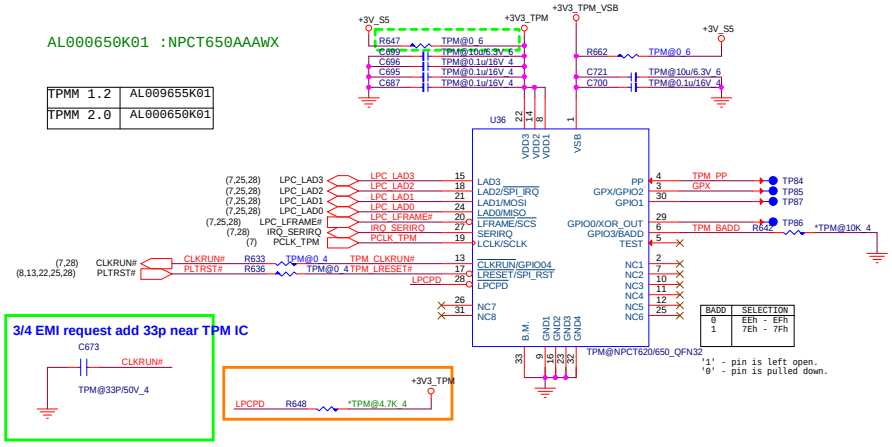
Spec define: High Active

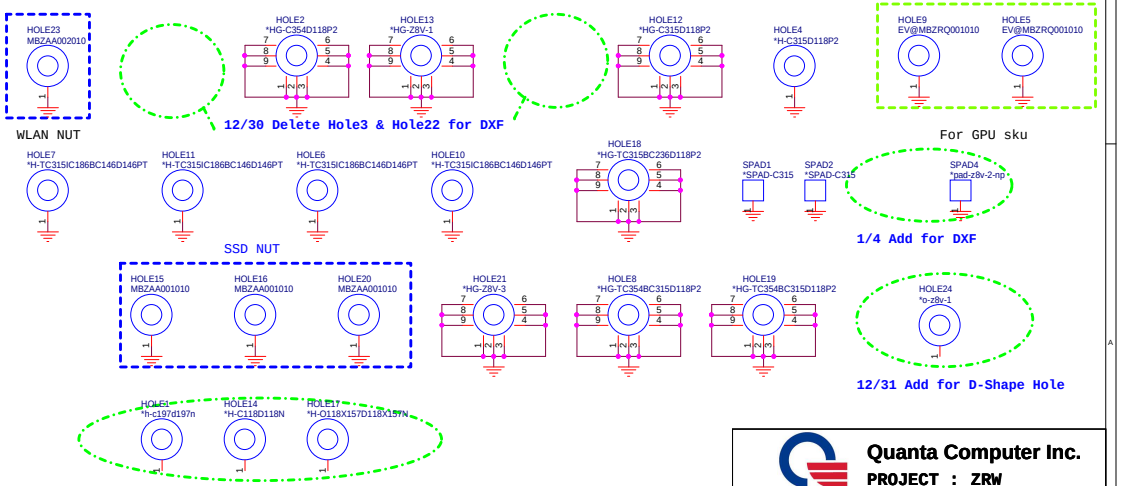
TPM NPCT650 (TPM)

SP@ BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAWX)

AL000650K01 :NPCT650AAAWX

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01





Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	1A
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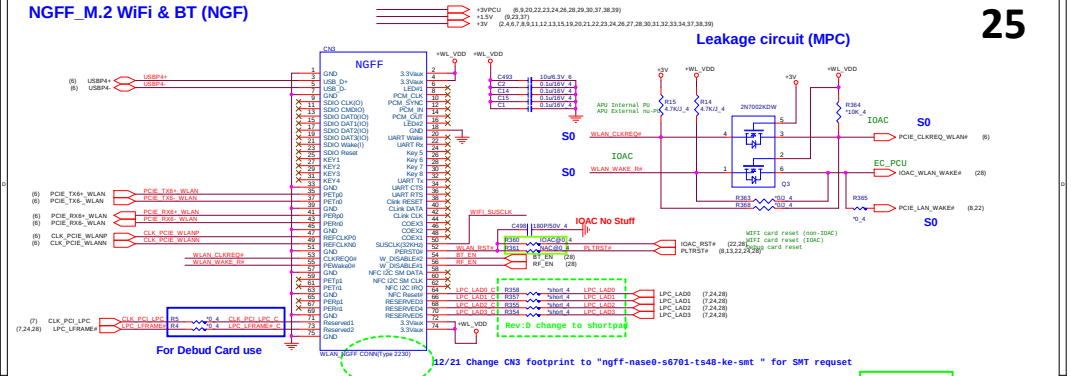
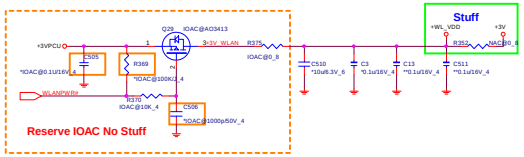
NGFF_M.2 WiFi & BT (NGF)



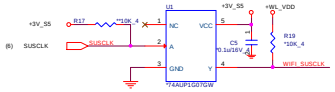
Leakage circuit (MPC)

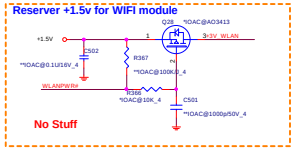
Low	Mini card +3V power enable
High	Mini card +3V power disable

(28) WLANPWR#

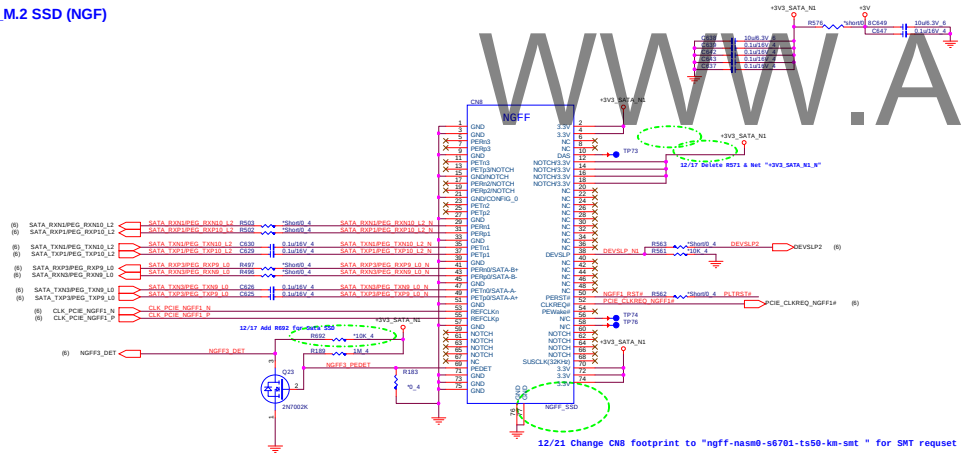


Reserve only for Intel module no need to stuff by default 11/24





NGFF_M.2 SSD (NGF)



Quanta Computer Inc.
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Size: Document Number: Mini-Card/WL3G/SIM Rev: 1A
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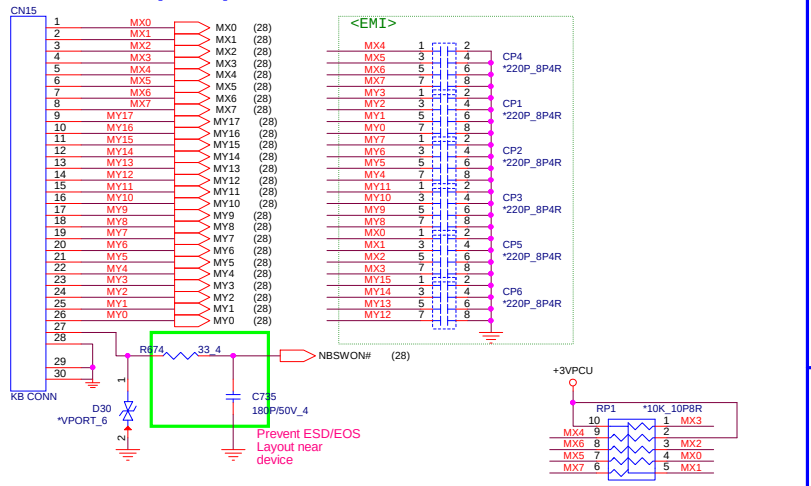
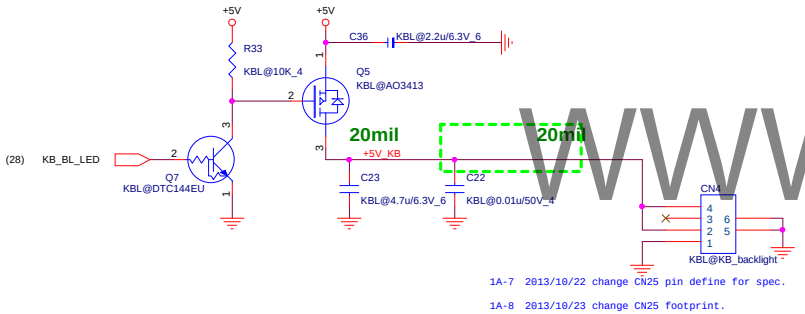
KEYBOARD (KBC)



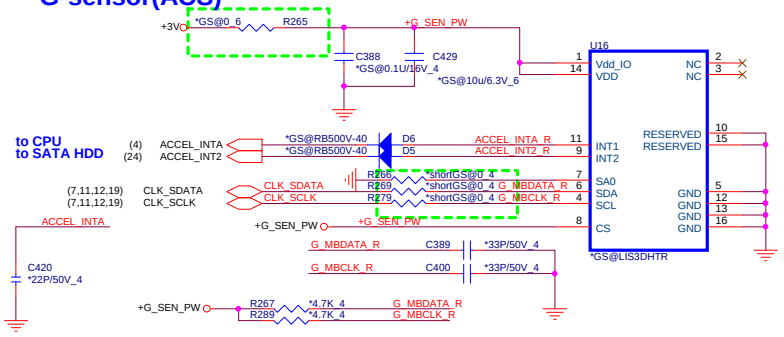
KB_BL LED (KBC)



1A-7 2013/10/22 change CN25 pin define for spec.

1A-8 2013/10/23 change CN25 footprint.

G-sensor(ACS)



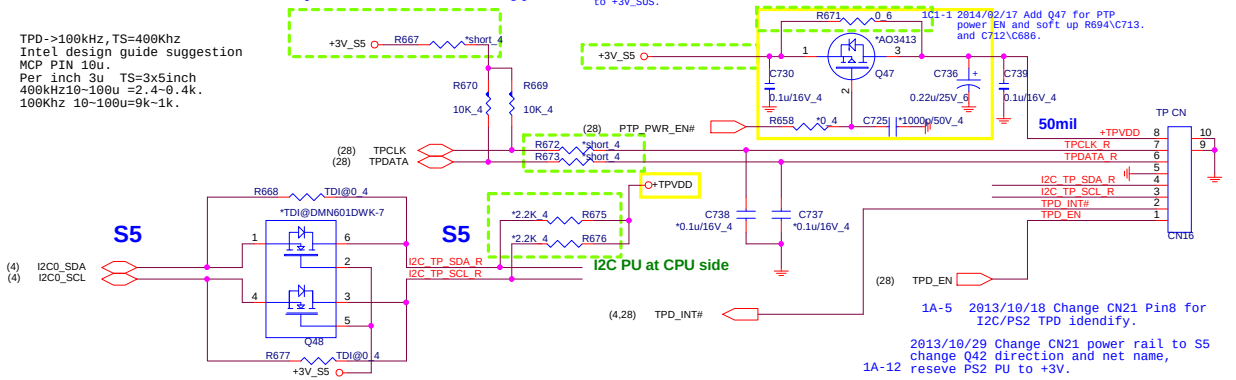
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.

1C-4 2014/01/15 reserve TP power rail +3V_S5.

1C1-1 2014/02/17 Add Q47 for PTP power EN and soft up R694\C713. and C712\C686.

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.



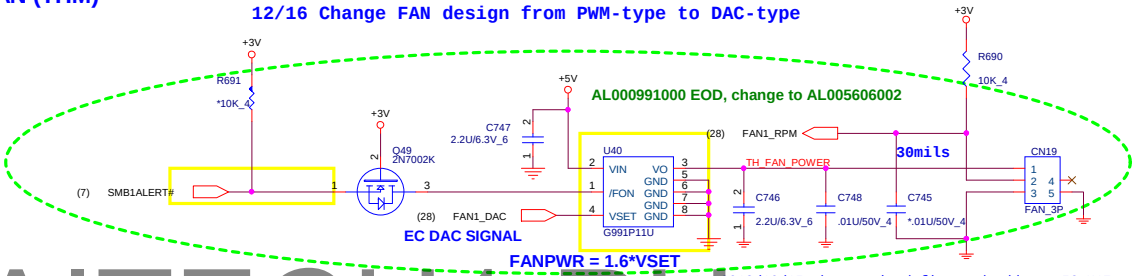
1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.

2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,

1A-12 reseve PS2 PU to +3V.

CPU FAN (THM)

12/16 Change FAN design from PWM-type to DAC-type



1A-12013/10/15 change pin define and add pwm IC U17.

1A-42013/10/17 Change U17 to G991P11U and PU U17 pin1.

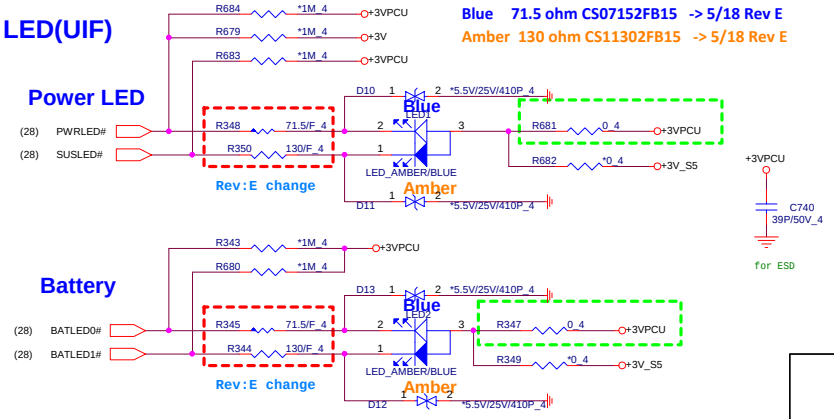
1A-92013/10/24 Add alert on U17.1 for CPU themal tempture.

1A-13 2013/10/31CN15 Pin2/3 swap.

POWER LED(UIF)

Blue 71.5 ohm CS07152FB15 -> 5/18 Rev E

Amber 130 ohm CS11302FB15 -> 5/18 Rev E



Quanta Computer Inc.

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	KB/TP/FAN	1A

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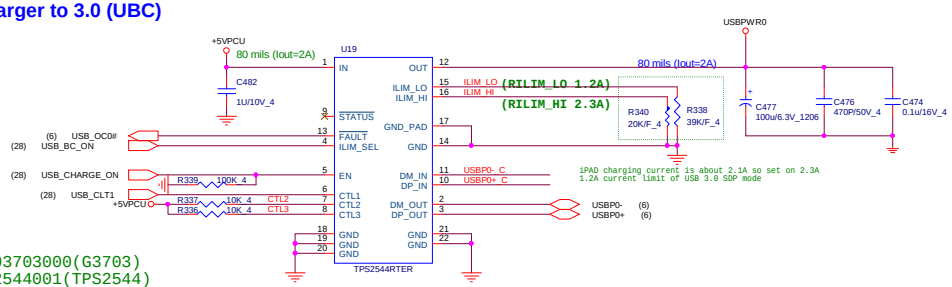
USB Charger to 3.0 (UBC)



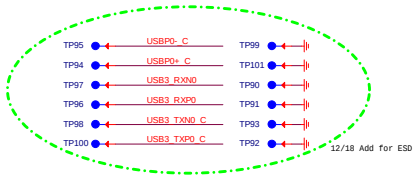
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

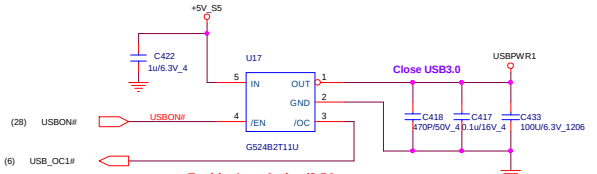
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

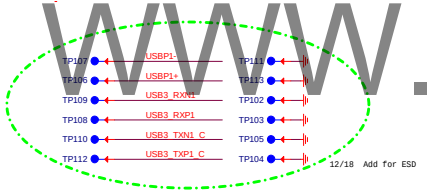
$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

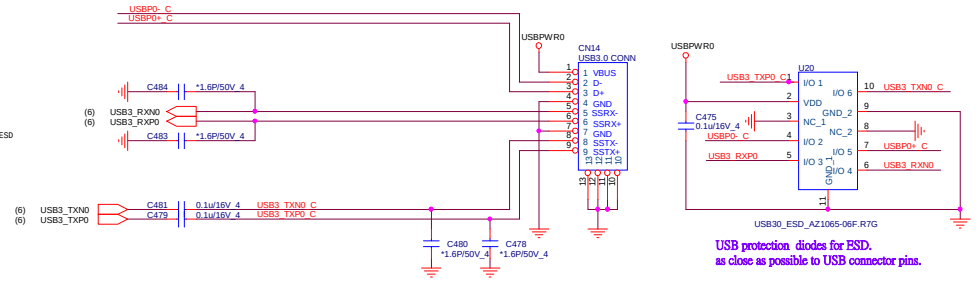
GMT:AL003703000(G3703)
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

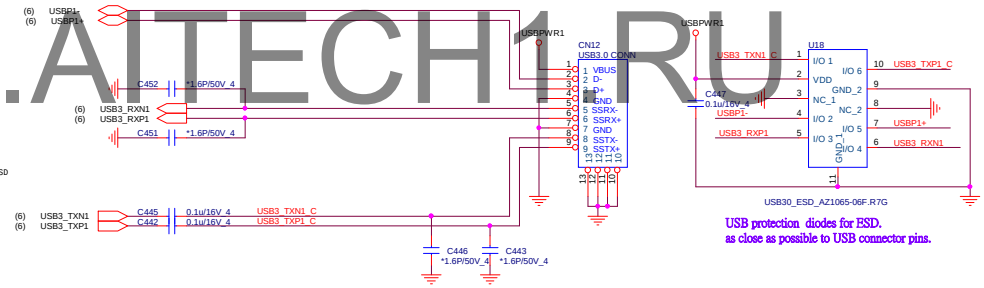
USB 3.0 Connector (UB3)



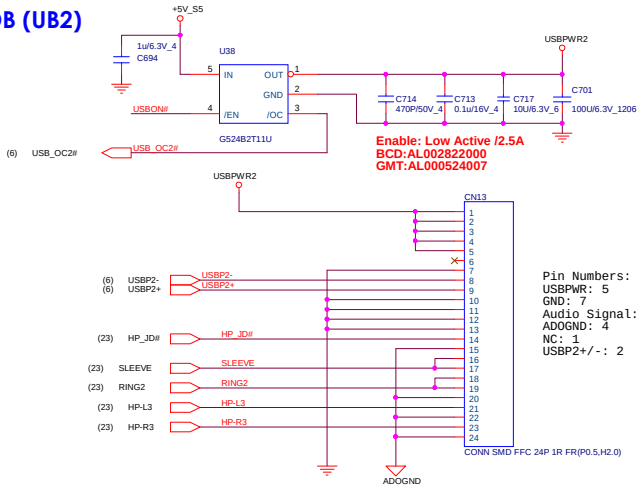




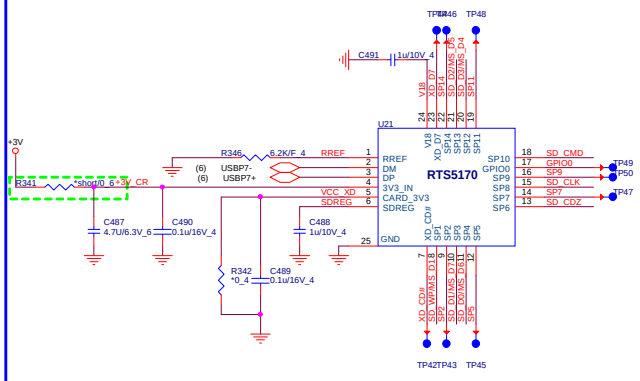


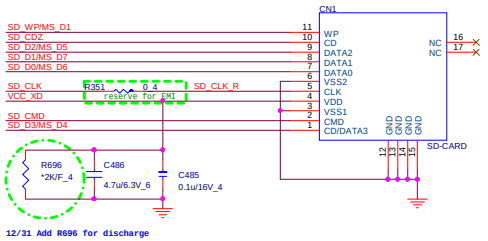


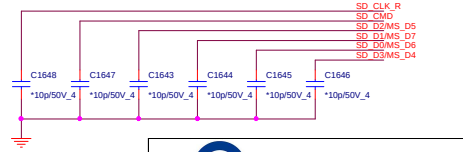
USB2.0 DB (UB2)



Card Reader (CRD)







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	USB3/Charger/CR/USB2 DB	1A

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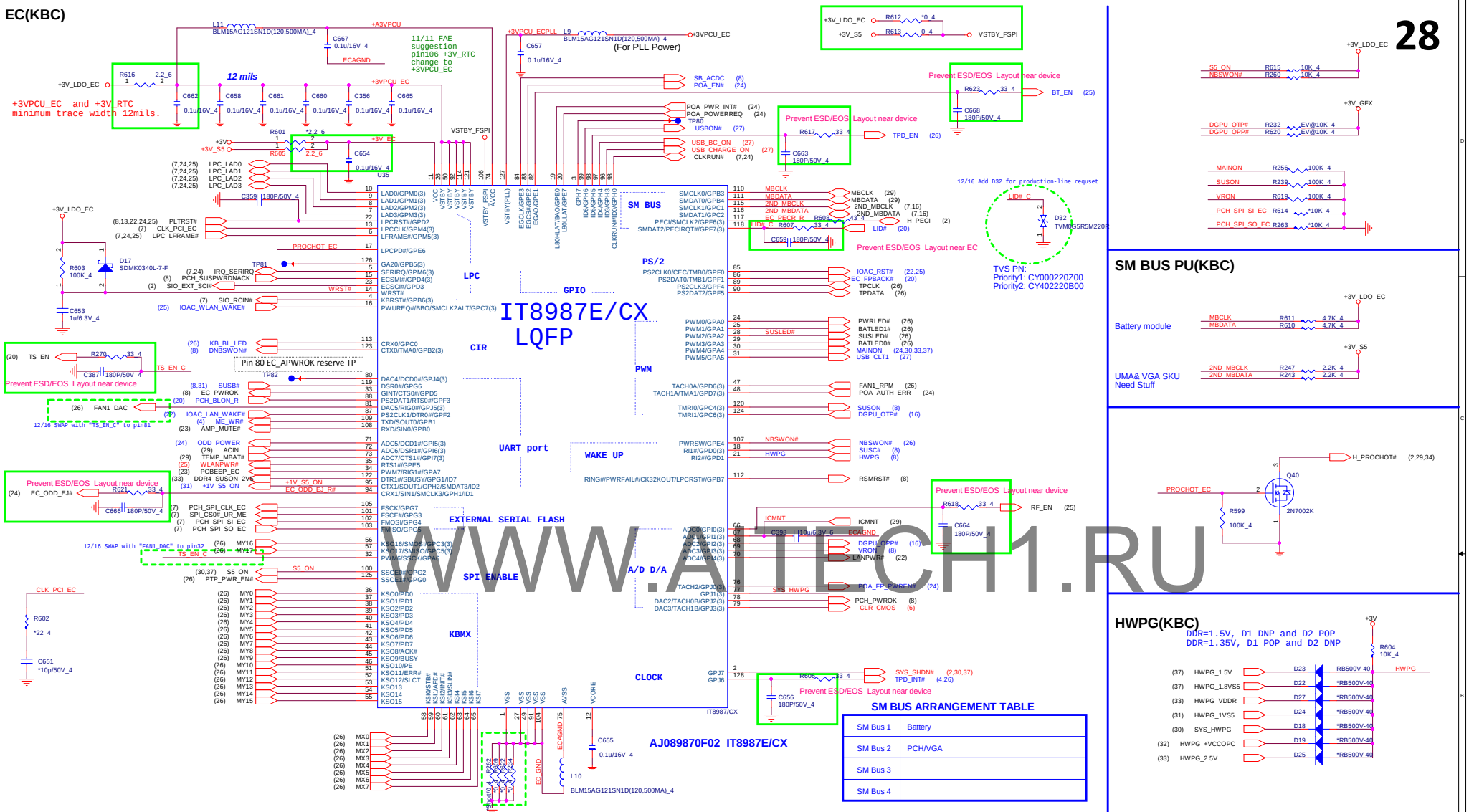
EC(KBC)



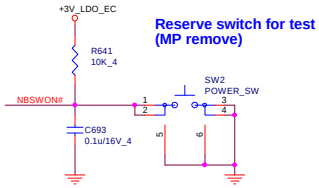
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

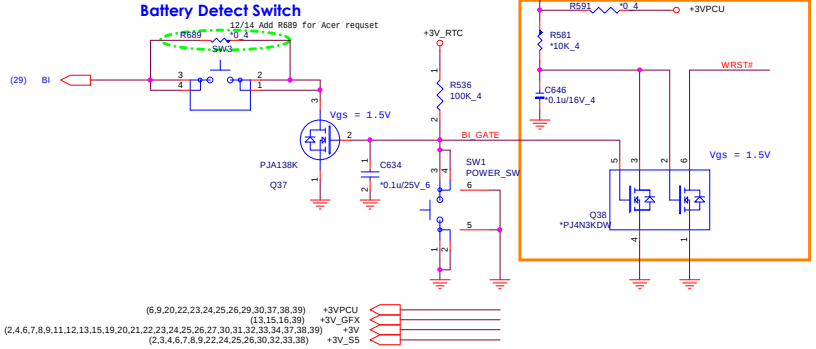
SM BUS PU(KBC)

HWPG(KBC)

Reserve switch for test (MP remove)



Reset SW (FSW)



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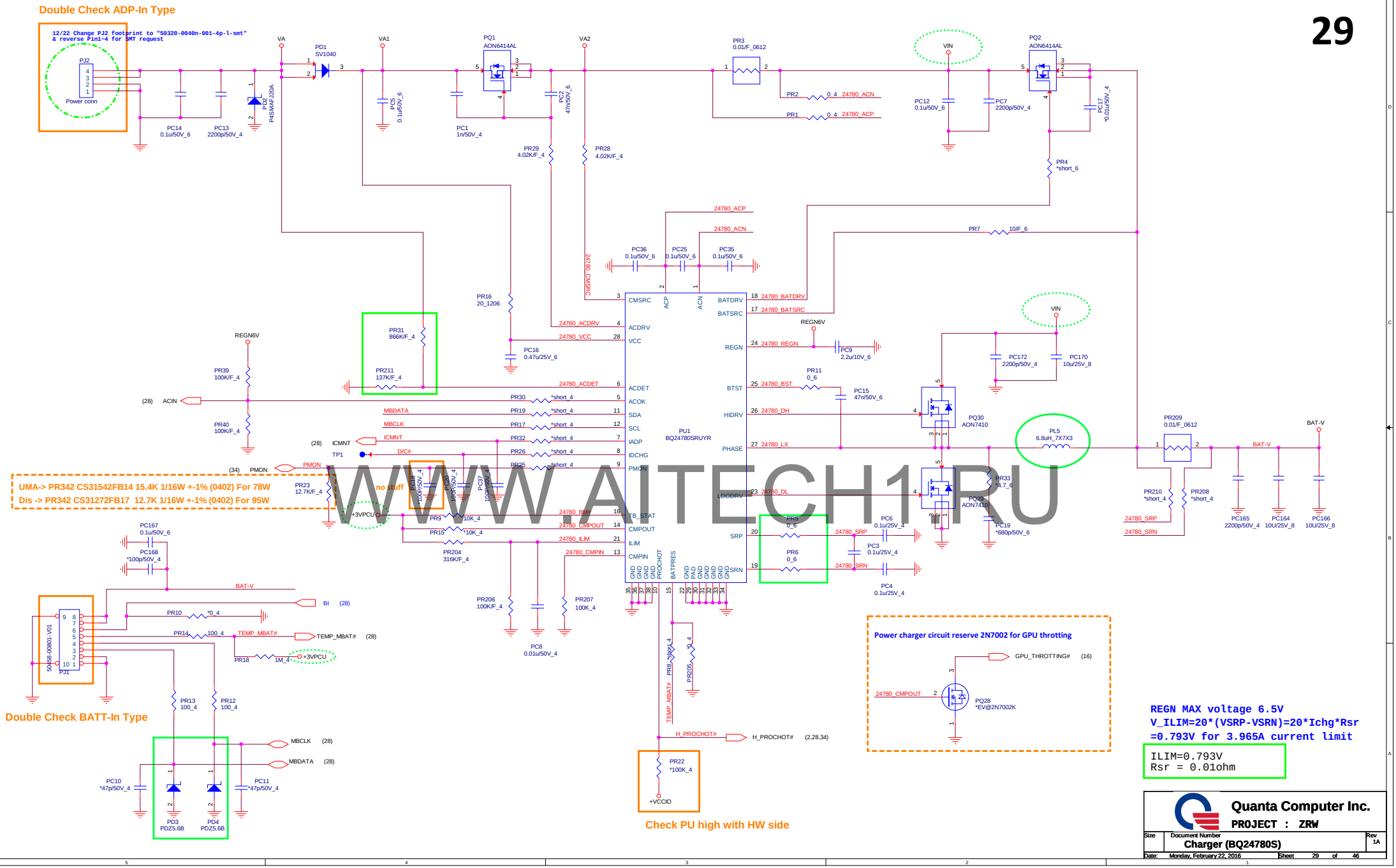
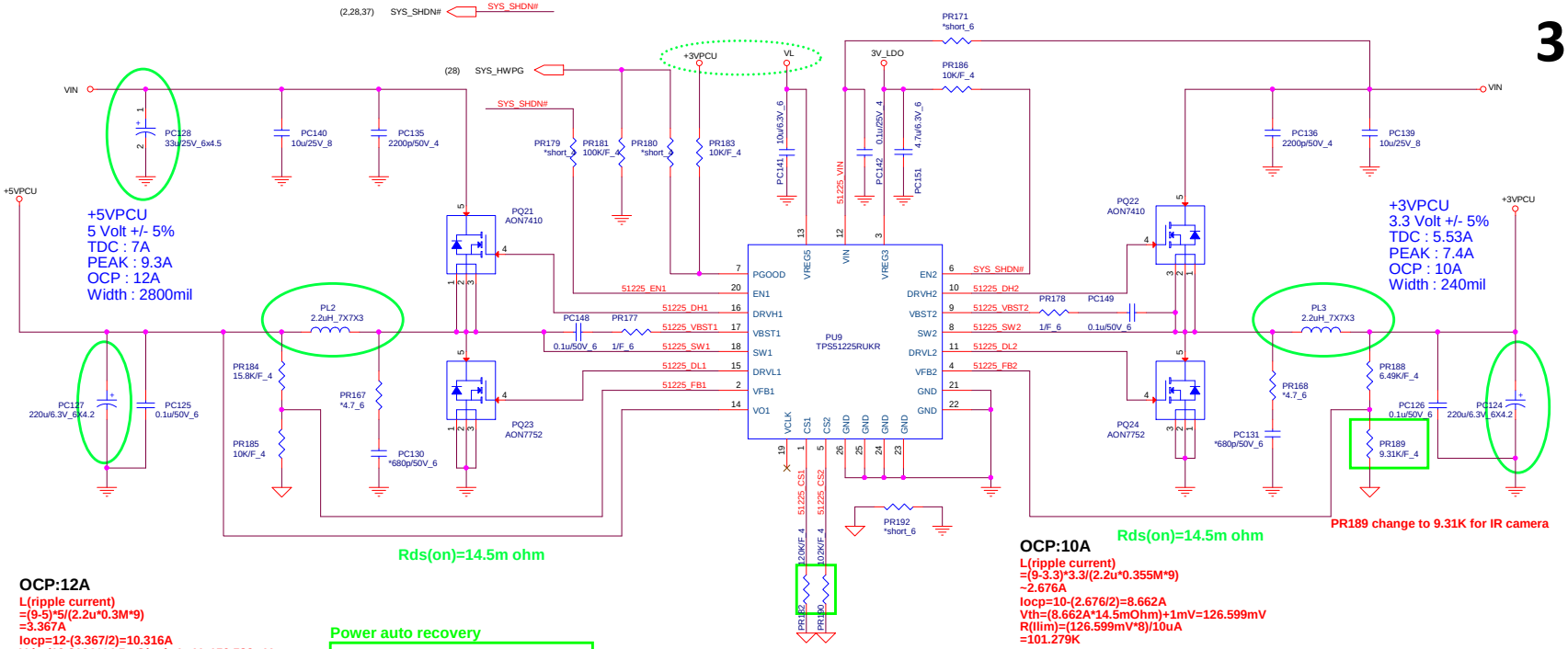




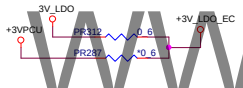
OCP:12A

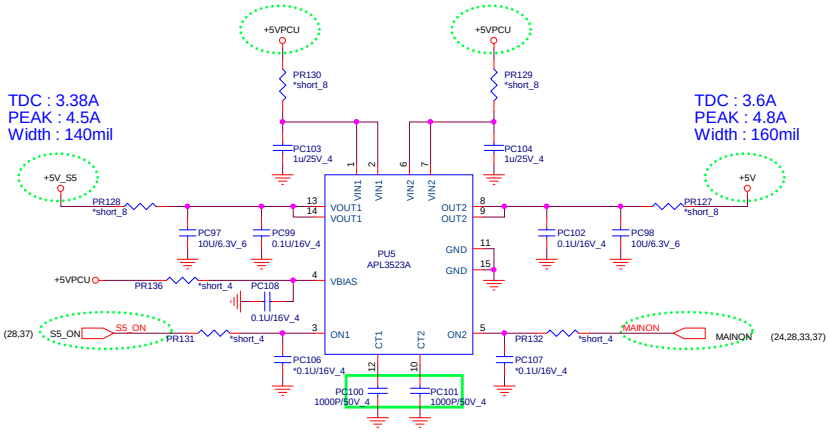
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=12-(3.367/2)=10.316A
Vth=(10.316A*14.5mOhm)+1mV=150.589mV
R(Ilim)=(150.589mV*8)/10uA
~120.47K

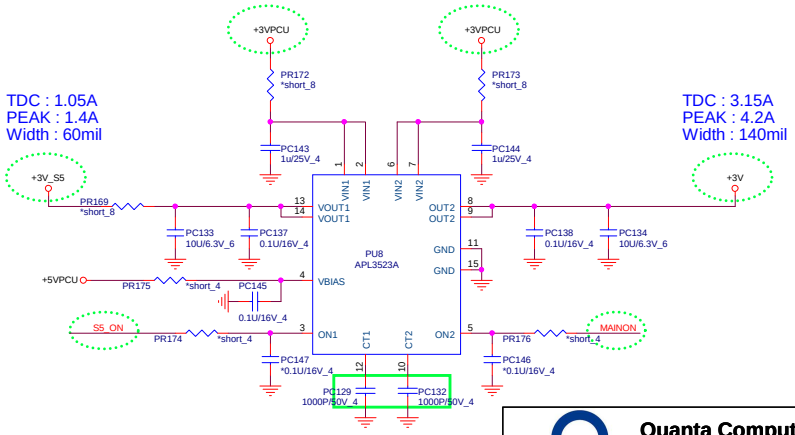
OCP:10A

L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=10-(2.676/2)=8.662A
Vth=(8.662A*14.5mOhm)+1mV=126.599mV
R(Ilim)=(126.599mV*8)/10uA
=101.279K

Power auto recovery







Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	SYSTEM 5V/3V (TPS51225R)	1A

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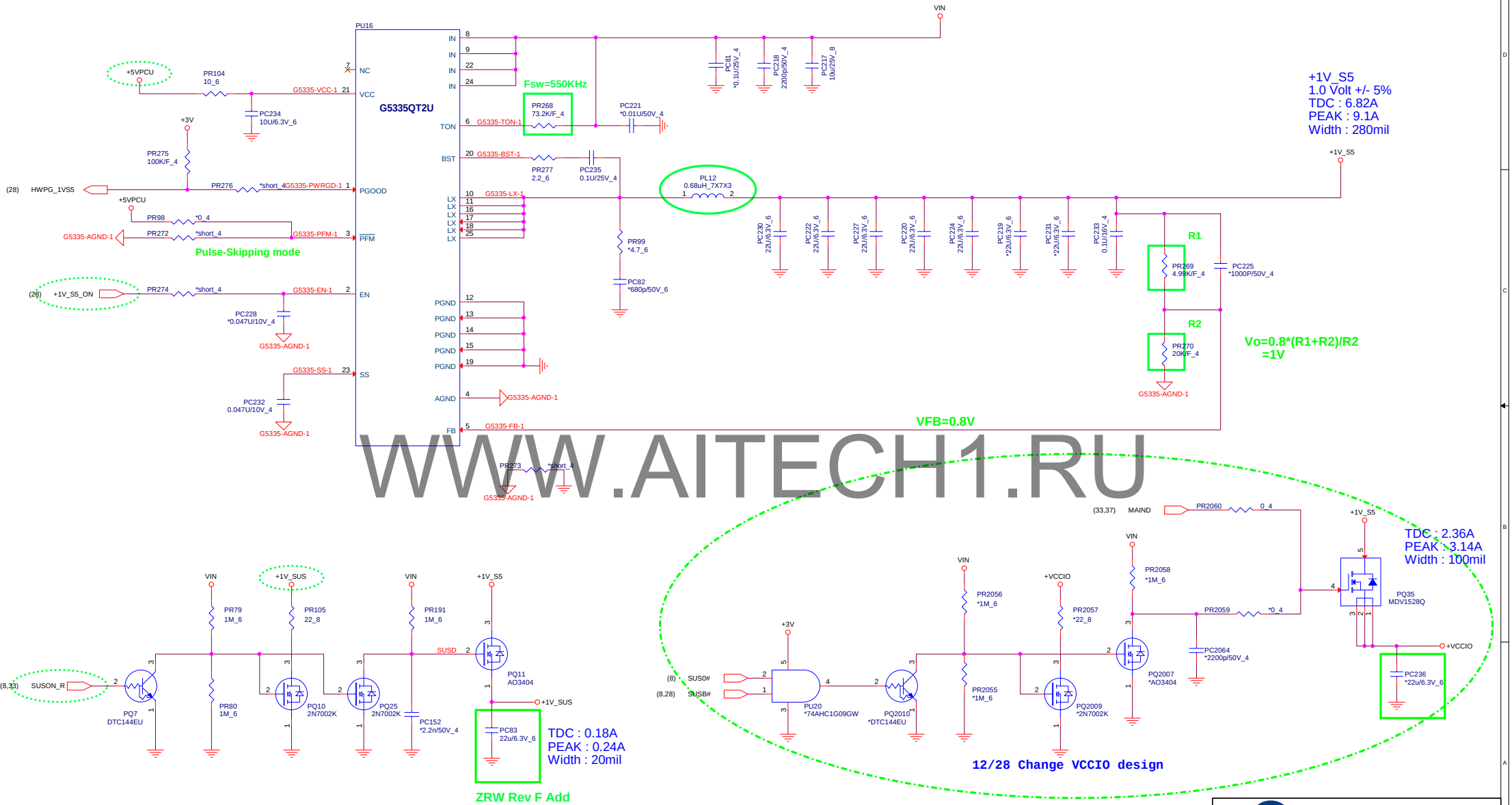

Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number	Rev
	+1V_S5 (G5335QT2U)	1A
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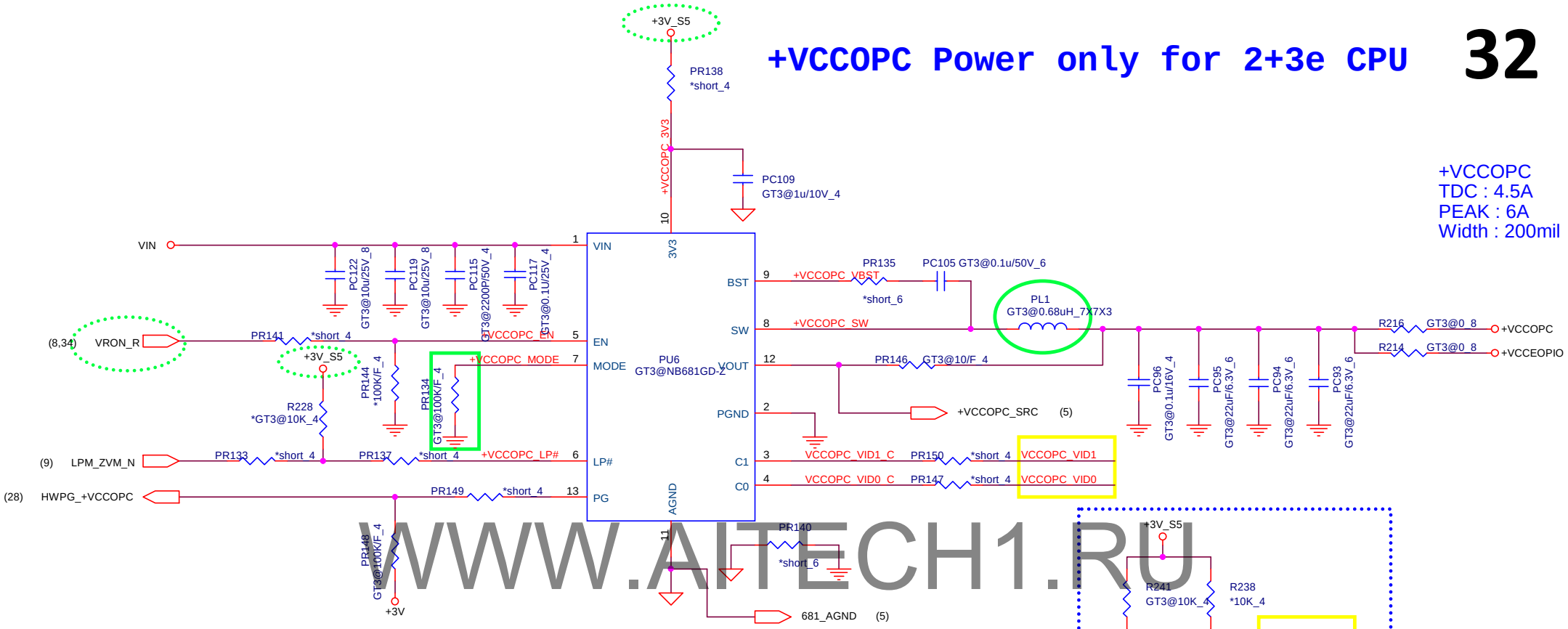
+VCCOPC Power only for 2+3e CPU

+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

(5) +VCCOPC
(20,23,24,29,30,31,33,34,35,36,37,38,39) VIN
(2,4,6,7,8,9,11,12,13,15,19,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39) +3V
(2,3,4,6,7,8,9,22,24,25,26,28,30,33,38) +3V_S5

Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	+VCCOPC (NB681GD-Z)	1A

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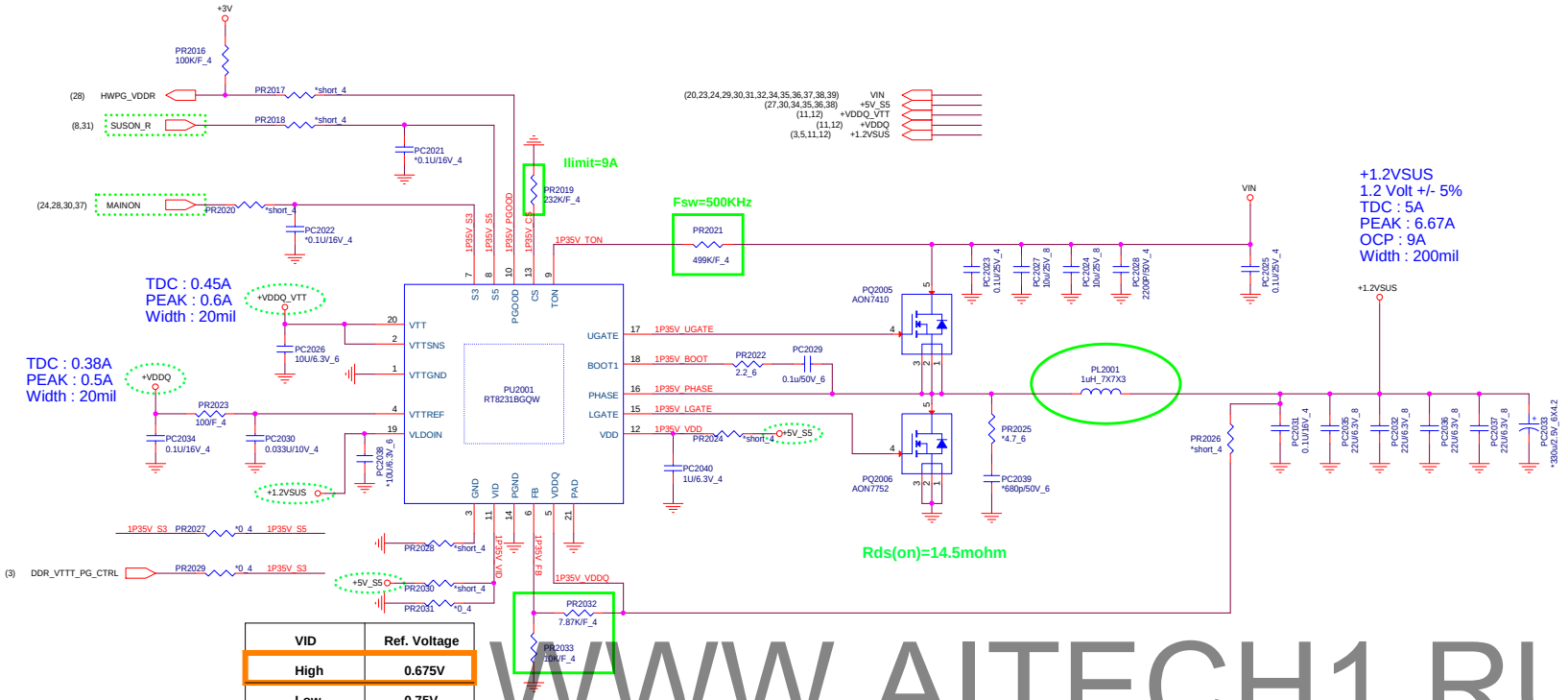


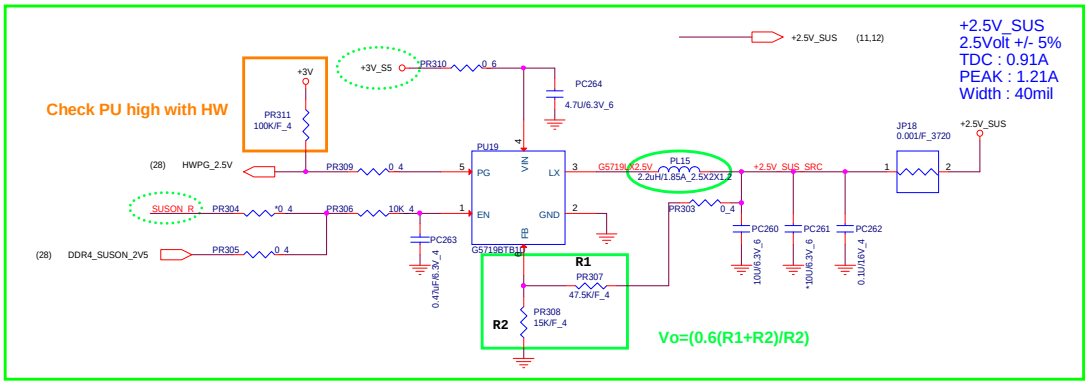
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=9A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=9-(2.248/2)*14.5mohm
=114.202mV
Rlimit=114.202mV/5uA*10=228.4Kohm

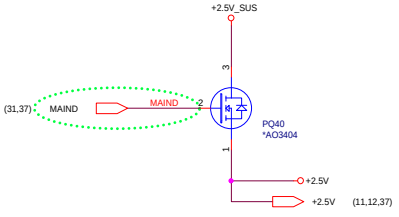
DDR=1.2V
PR2032=7.87K/F_4
PR2033=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

+2.5VSUS Power Rail For DDR4



10/26 Reserve +2.5V for DDR4 VDDSPD



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	DDR4_+1.2VSUS (G5316RZ1D)	1A

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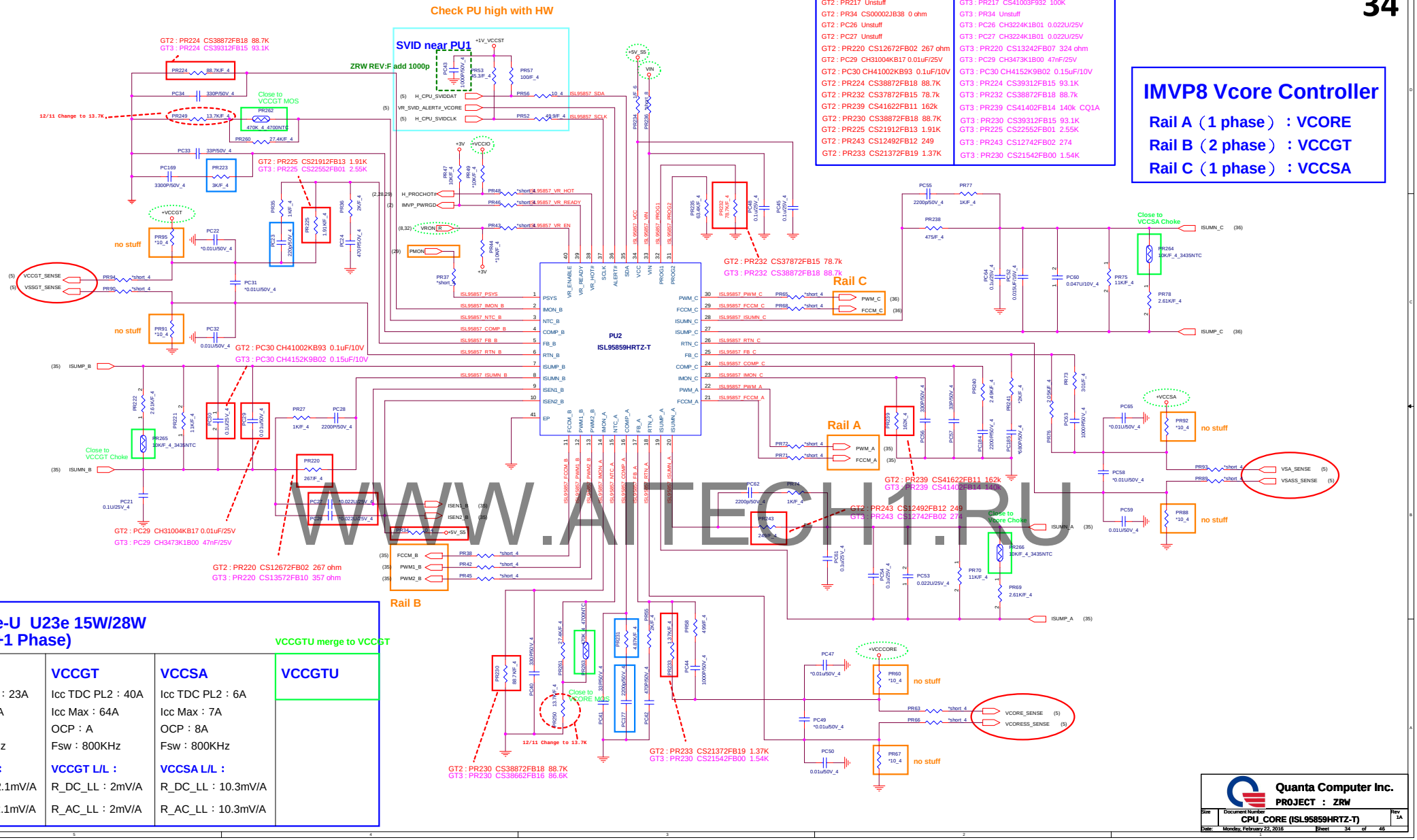

GT2 : PR217 Unstuff	GT3 : PR217 CS41003F932 100K
GT2 : PR34 CS00002JB38 0 ohm	GT3 : PR34 Unstuff
GT2 : PC26 Unstuff	GT3 : PC26 CH3224K1B01 0.022U/25V
GT2 : PC27 Unstuff	GT3 : PC27 CH3224K1B01 0.022U/25V
GT2 : PR220 CS12672FB02 267 ohm	GT3 : PR220 CS13242FB07 324 ohm
GT2 : PC29 CH31004KB17 0.01uF/25V	GT3 : PC29 CH3473K1B00 47nF/25V
GT2 : PC30 CH41002KB93 0.1uF/10V	GT3 : PC30 CH4152K9B02 0.15uF/10V
GT2 : PR224 CS38872FB18 88.7K	GT3 : PR224 CS39312FB15 93.1K
GT2 : PR232 CS37872FB15 78.7k	GT3 : PR232 CS38872FB18 88.7k
GT2 : PR239 CS41622FB11 162k	GT3 : PR239 CS41402FB14 140k CQ1A
GT2 : PR230 CS38872FB18 88.7K	GT3 : PR230 CS39312FB15 93.1K
GT2 : PR225 CS21912FB13 1.91K	GT3 : PR225 CS22552FB01 2.55K
GT2 : PR243 CS12492FB12 249	GT3 : PR243 CS12742FB02 274
GT2 : PR233 CS21372FB19 1.37K	GT3 : PR230 CS21542FB00 1.54K

IMVP8 Vcore Controller

- Rail A（1 phase）：VCORE
- Rail B（2 phase）：VCCGT
- Rail C（1 phase）：VCCSA

Skylake-U U23e 15W/28W (1+2+1+1 Phase)

VCORE	VCCGT	VCCSA	VCCGTU
Icc TDC PL2：23A	Icc TDC PL2：40A	Icc TDC PL2：6A	
Icc Max：32A	Icc Max：64A	Icc Max：7A	
OCP：35A	OCP：A	OCP：8A	
Fsw：800KHz	Fsw：800KHz	Fsw：800KHz	
VCORE L/L：	**VCCGT L/L：**	**VCCSA L/L：**	
R_DC_LL：2.1mV/A	R_DC_LL：2mV/A	R_DC_LL：10.3mV/A	
R_AC_LL：2.1mV/A	R_AC_LL：2mV/A	R_AC_LL：10.3mV/A	

Quanta Computer Inc.
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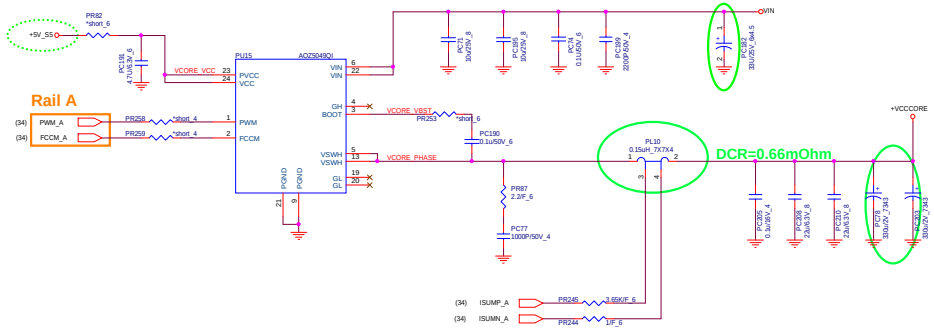
GT2 : PR19 Unstuff	GT3 : PR19 CS41003F932 100K

VCORE



VCORE

Icc TDC PL2：23A

Icc Max：29A

OCP：35A

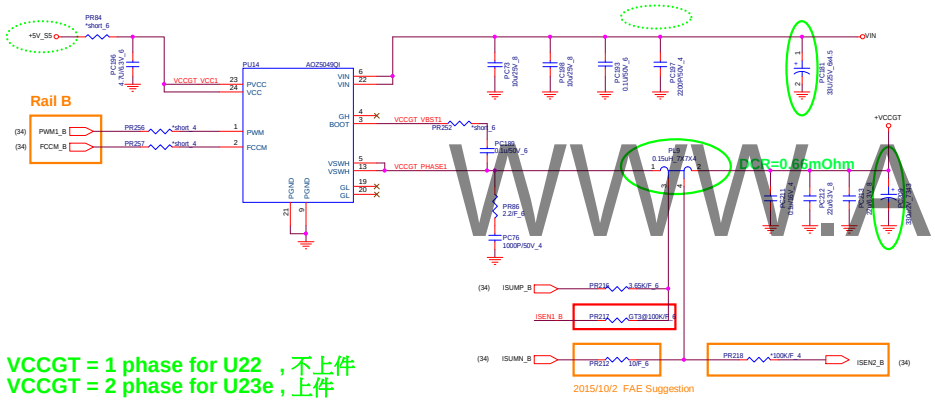
Fsw：800KHz

VCORE L/L：

R_DC_LL：2.1mV/A

R_AC_LL：2.1mV/A

VCCGT



VCCGT

Icc TDC PL2：40A

Icc Max：64A

OCP：A

Fsw：800KHz

VCCGT L/L：

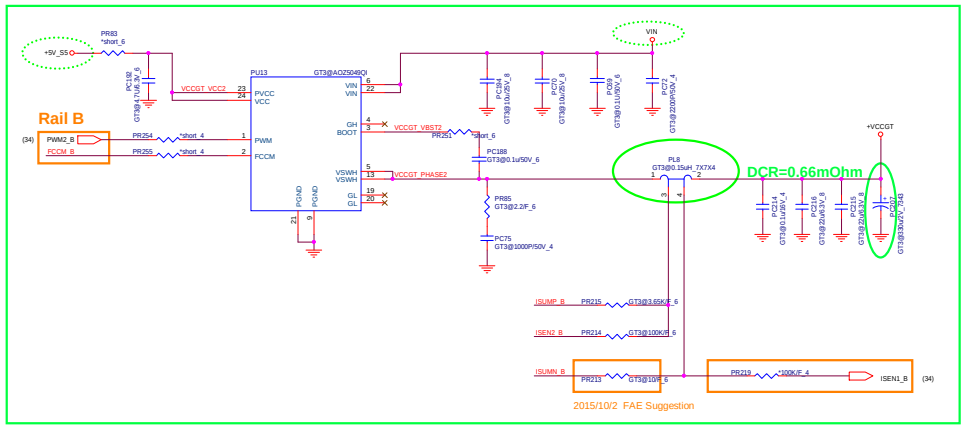
R_DC_LL：2mV/A

R_AC_LL：2mV/A

VCCGT = 1 phase for U22 ，不上件

VCCGT = 2 phase for U23e，上件

2015/10/2 FAE Suggestion



2015/10/2 FAE Suggestion

(5,34) +VCCCORE
(20,23,24,29,30,31,32,33,34,36,37,38,39) VIN
(5,34) +VCCGT
(27,30,33,34,36,38) +5V_S5

Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	VCORE/VCCGT (ISL95808HRZ-T)	1A
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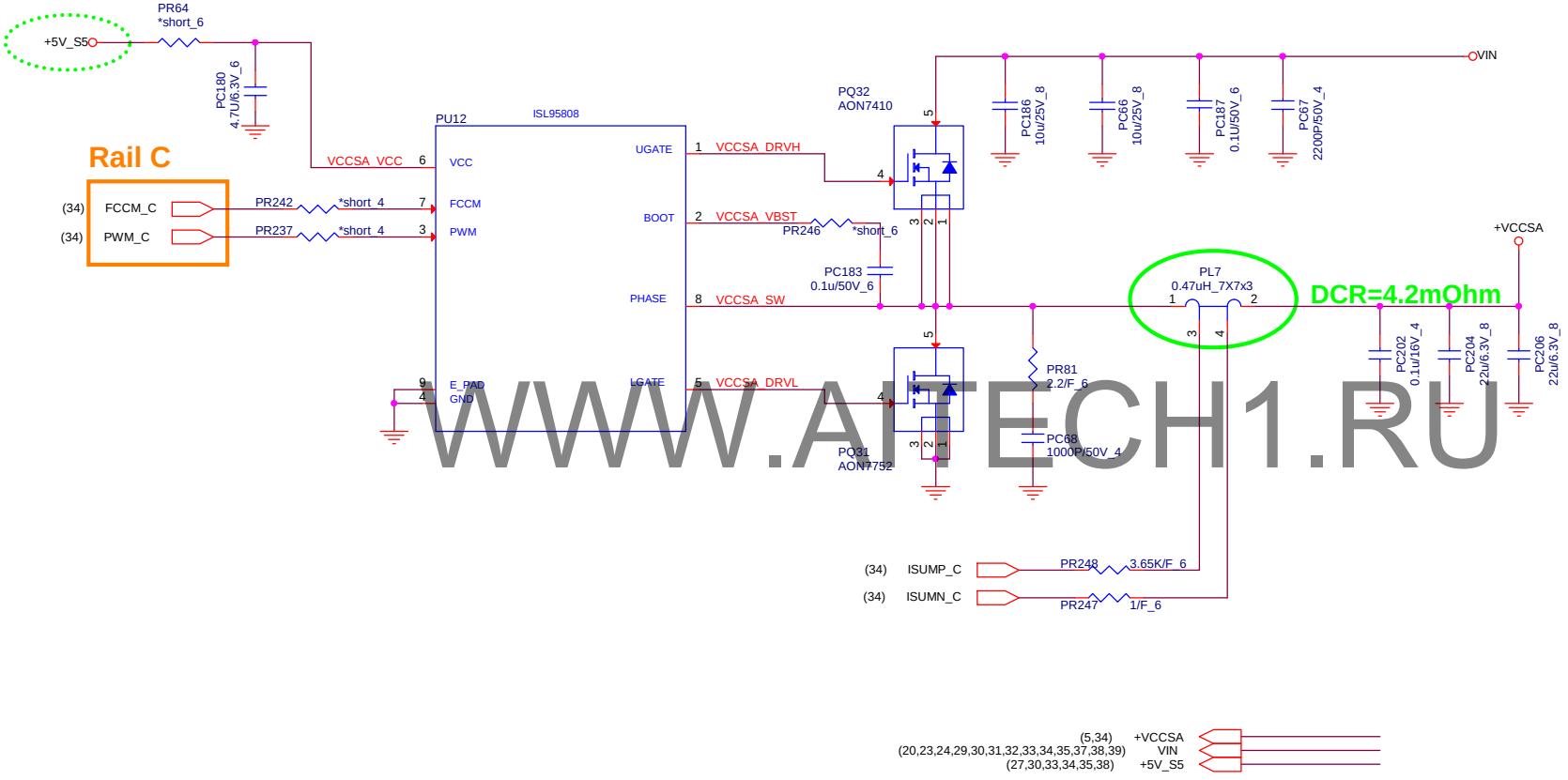
VCCSA



VCCSA

Icc TDC PL2：5A

Icc Max：5A

OCP：6A

Fsw：800KHz

VCCSA L/L：

R_DC_LL：10.3mV/A

R_AC_LL：10.3mV/A

Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: VCCSA (ISL95808HRZ-T)	Rev: 1A
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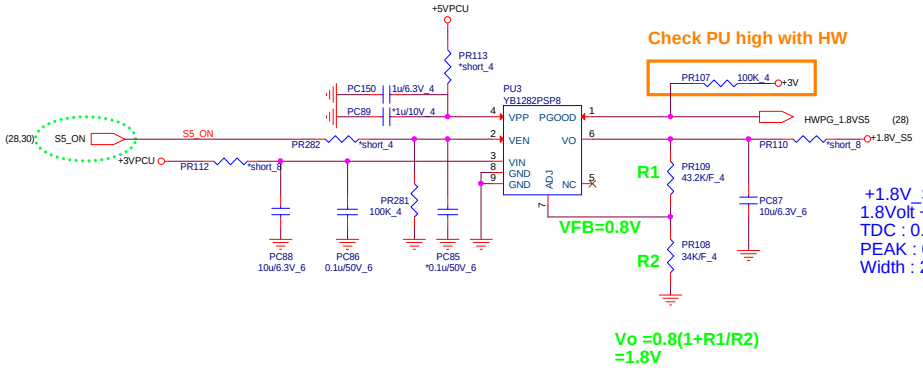
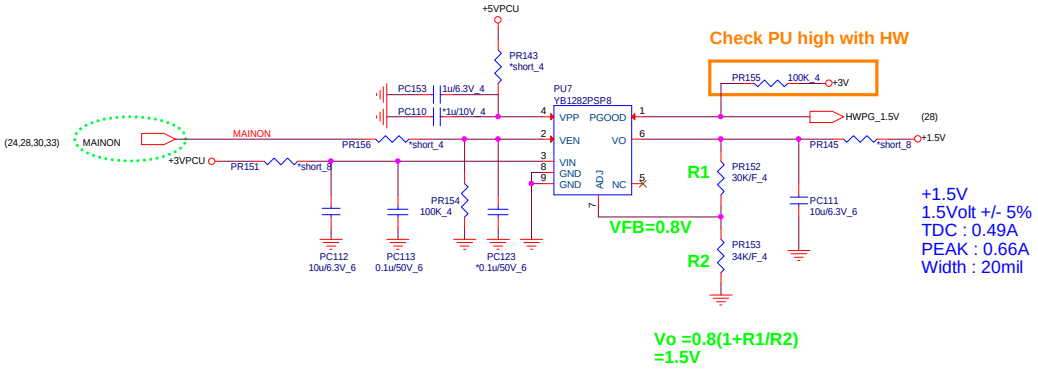
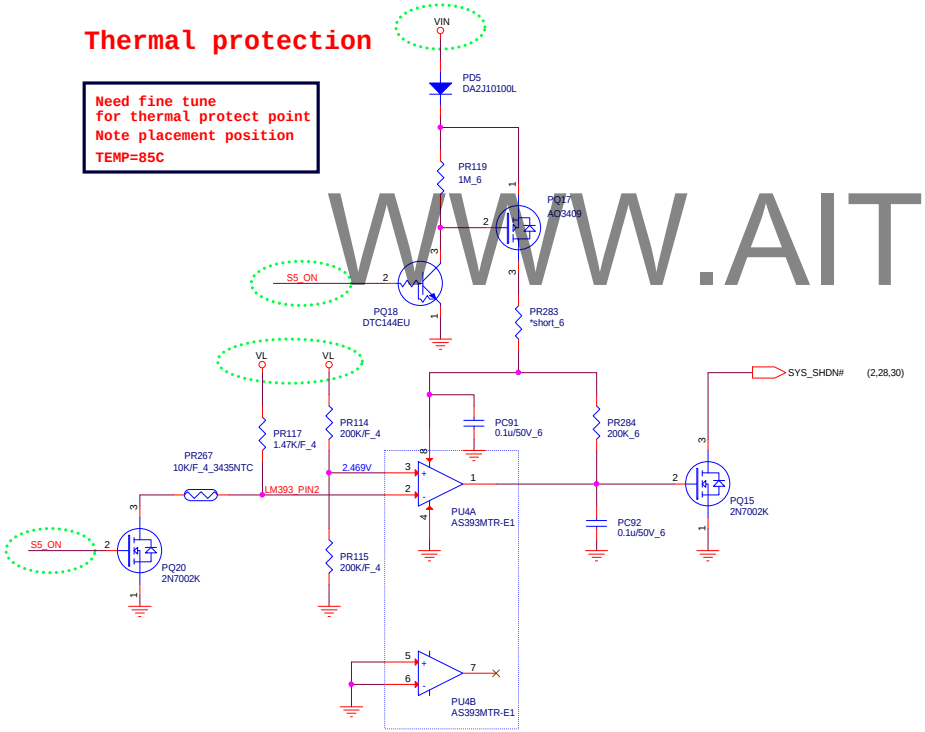




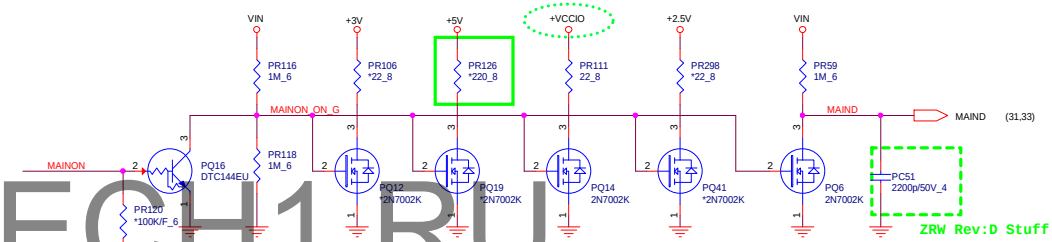
Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C



For EC control thermal protection (output 3.3V)

PR153 Change to
220 ohm for bo bo
sound issue.



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A

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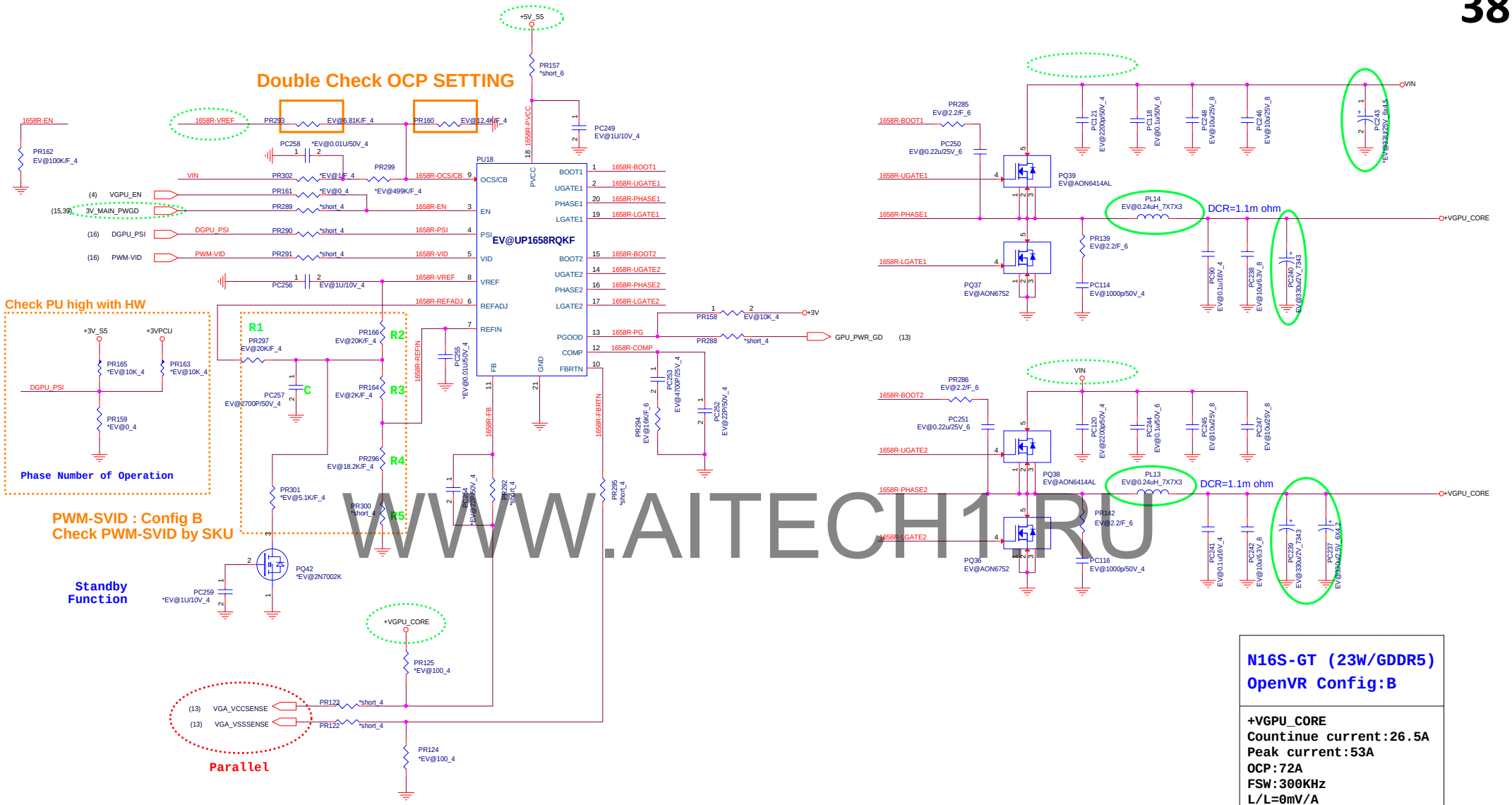
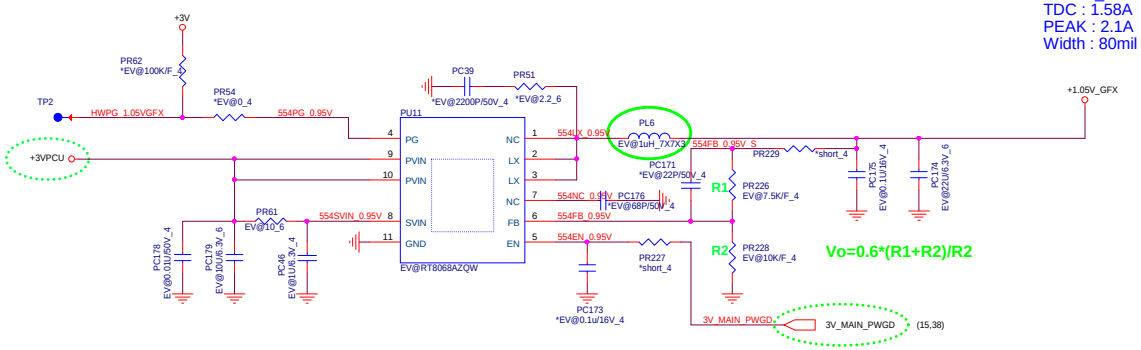
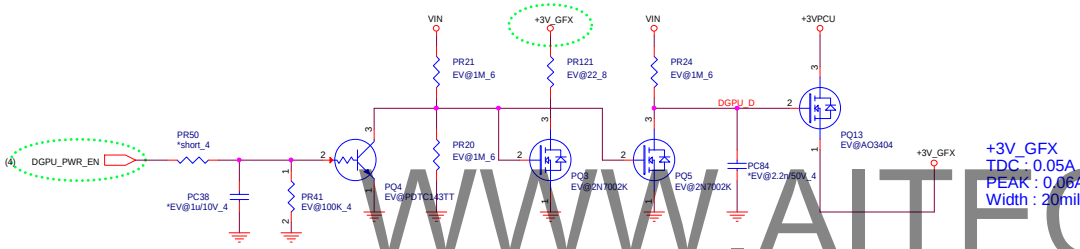


+1.05V_GFX
TDC : 1.58A
PEAK : 2.1A
Width : 80mil

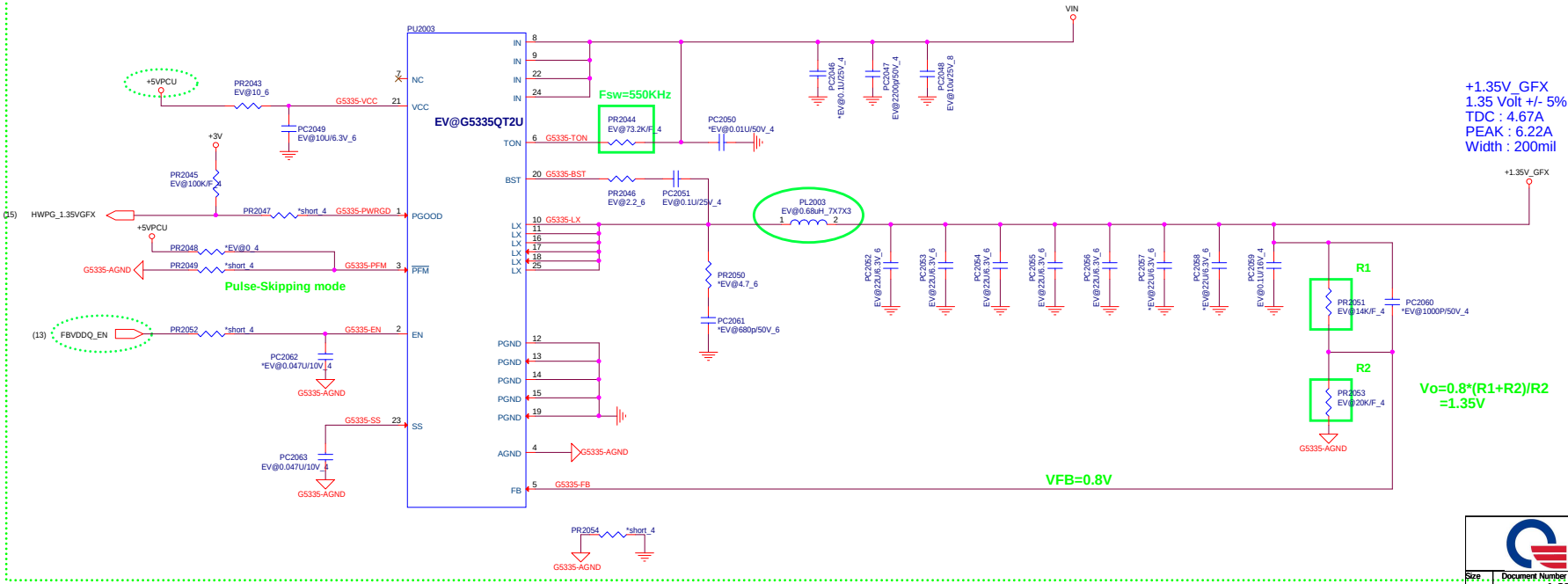


+3V_GFX
TDC : 0.05A
PEAK : 0.06A
Width : 20mil



+1.35V_GFX for GDDR5

+1.35V_GFX
1.35 Volt +/- 5%
TDC : 4.67A
PEAK : 6.22A
Width : 200mil



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	+1.35V_GFX/+1.05V_GFX/+3V_GFX	1A
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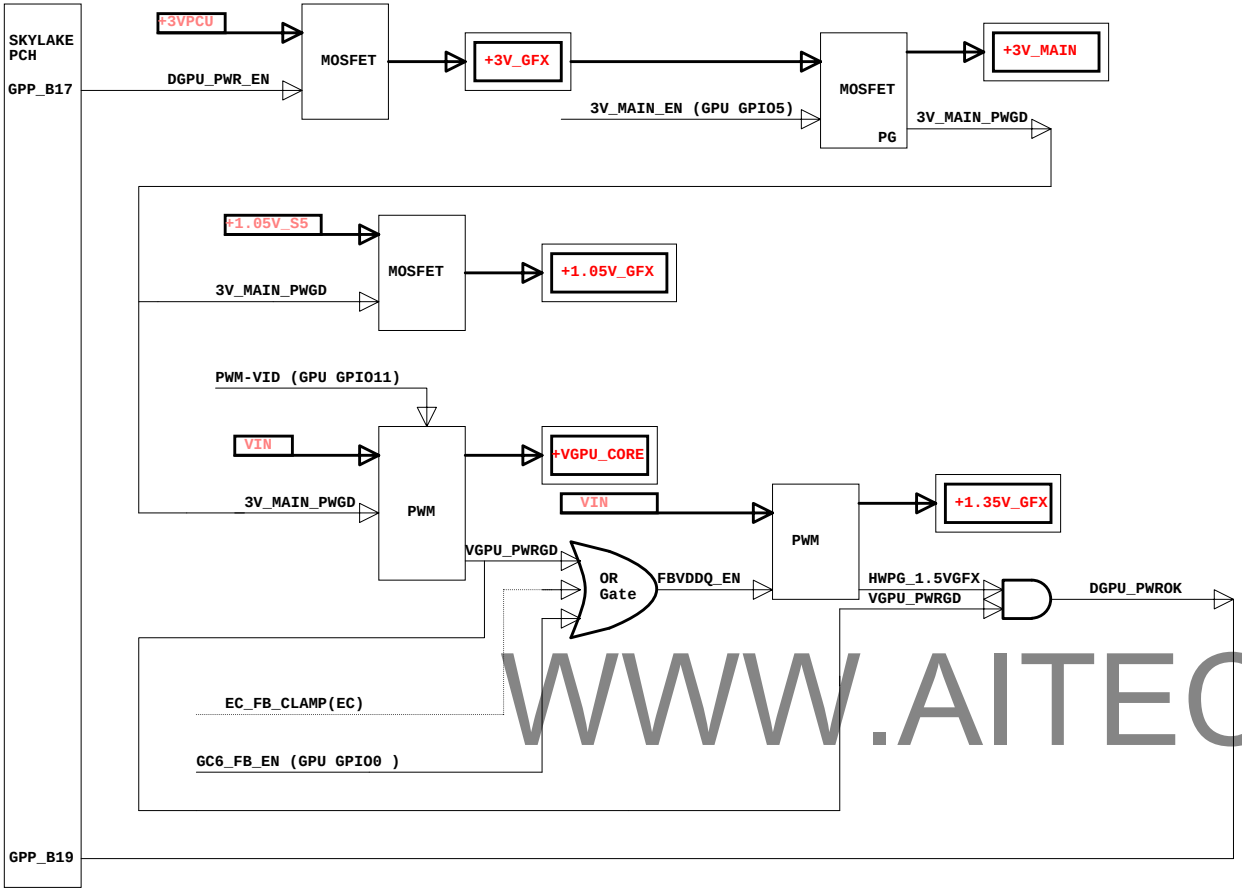
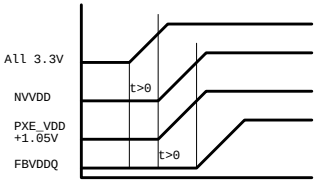
VGA power up sequence

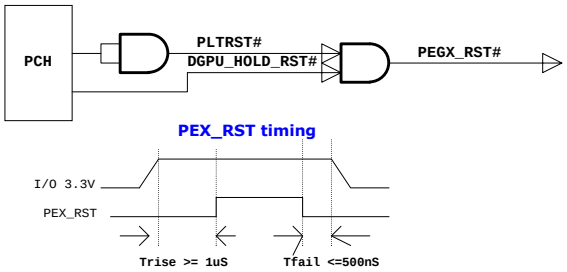




N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

VGA Reset



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	GPU PWR CRL	1A

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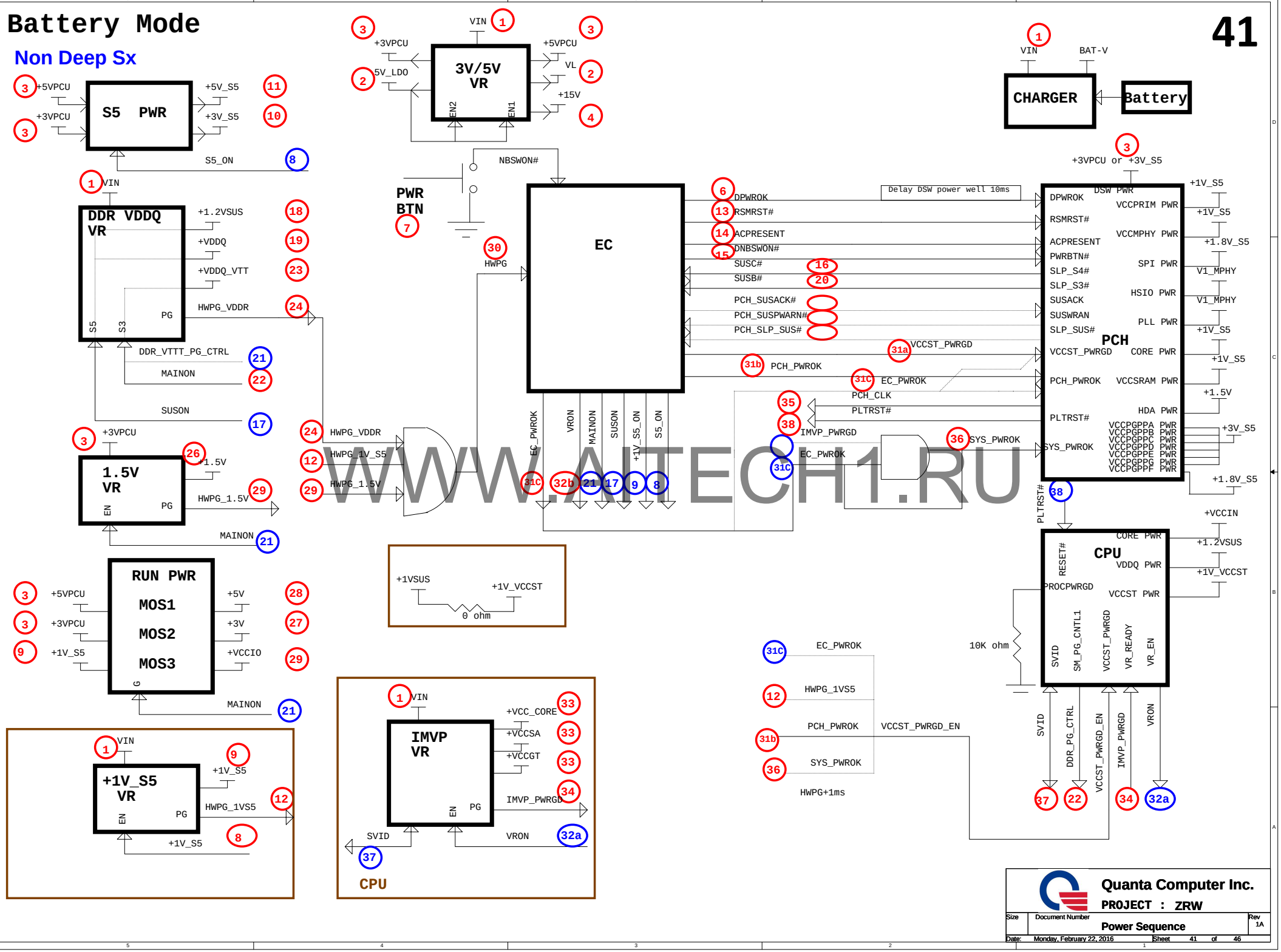
Battery Mode

Non Deep Sx



Quanta Computer Inc.	
PROJECT : ZRW	
Size	Document Number: Power Sequence
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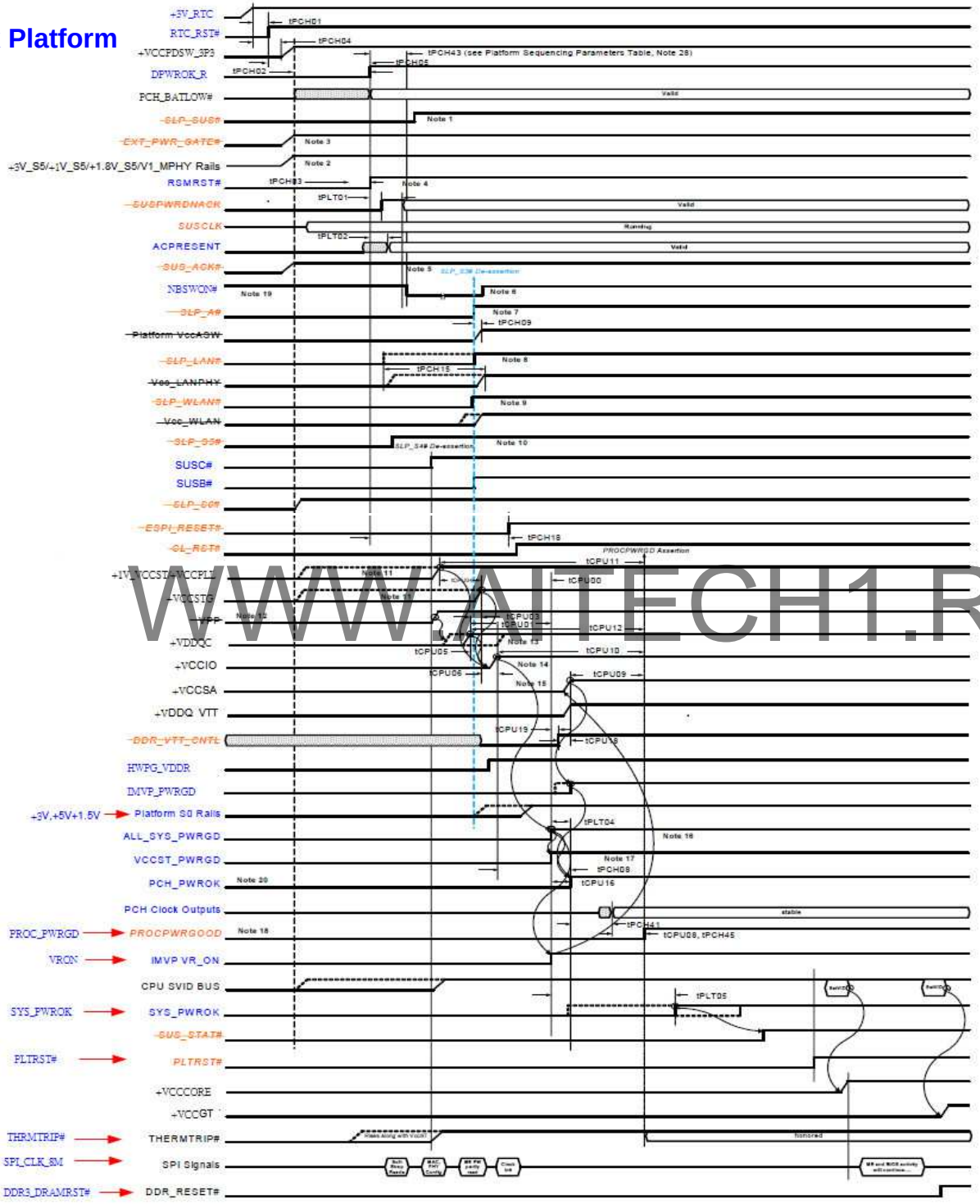
Skylake U Non-Deep Sx Platform Power on sequence



Quanta Computer Inc.	PROJECT : ZRW	
Size	Document Number: Power on Sequence	Rev 1A
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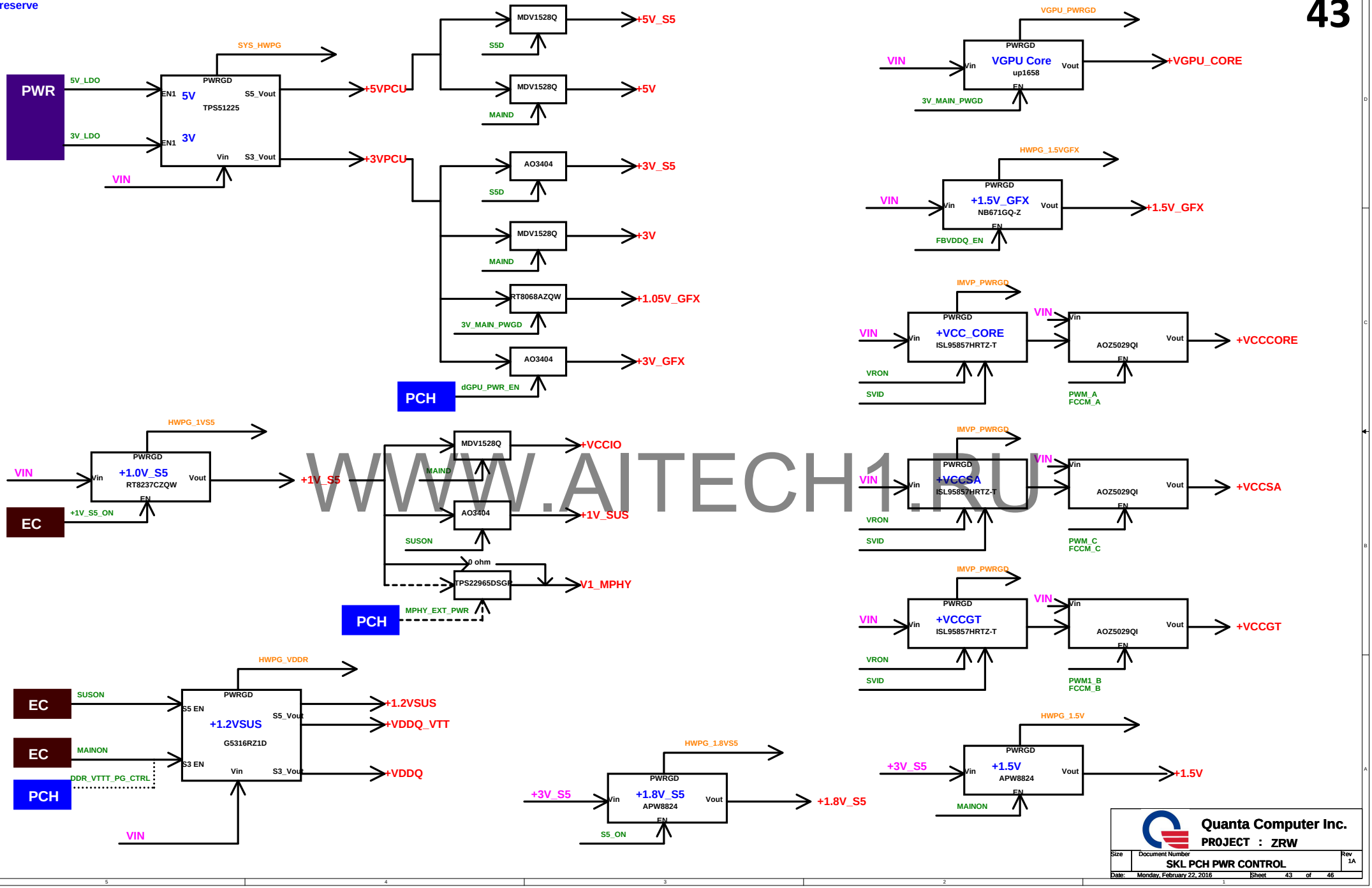
實線表default
虛線表reserve



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	SKL PCH PWR CONTROL	1A
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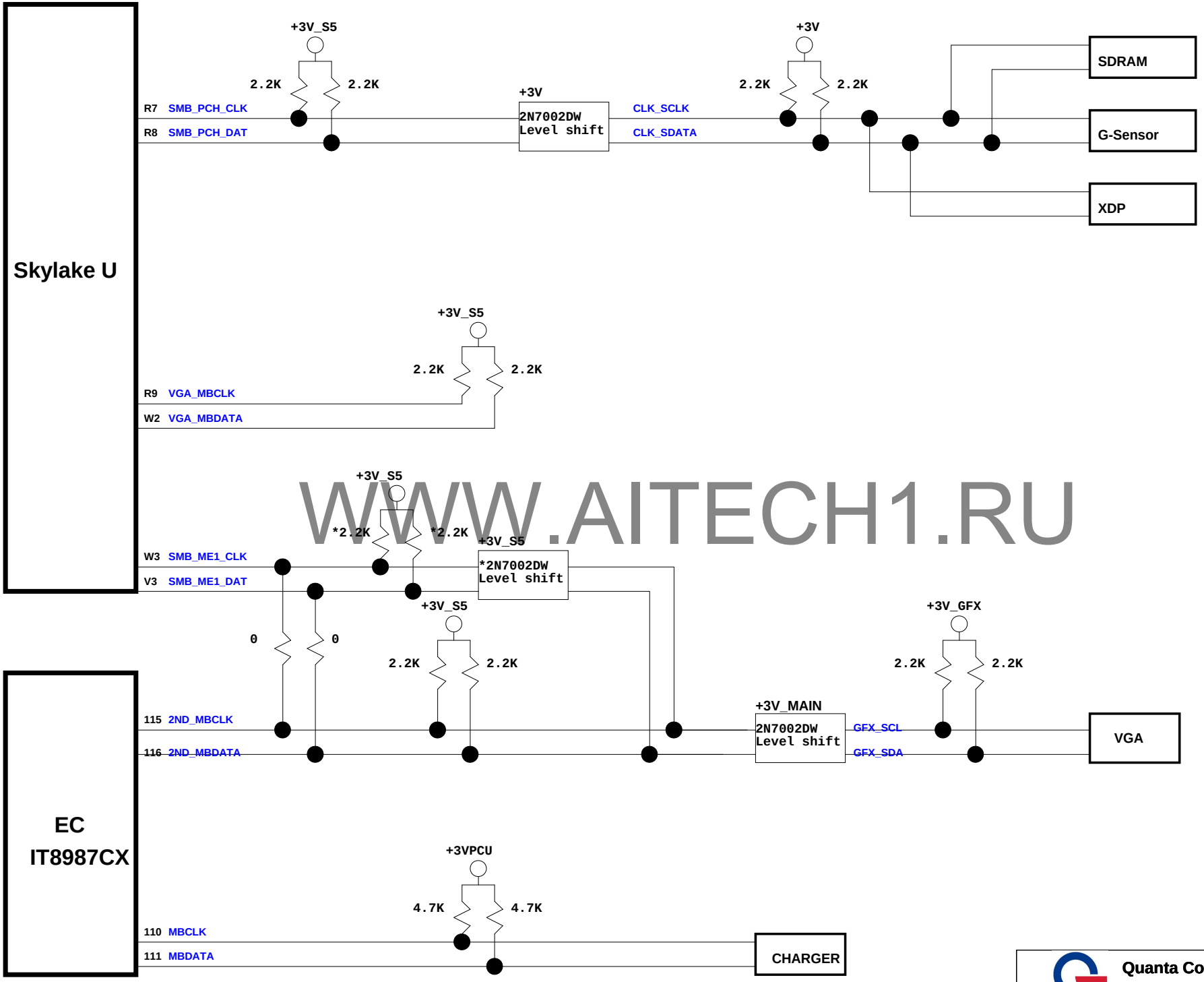

Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	SMBUS Block Diagram	1A
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